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GENERATION OF PROGRAMMABLE COMPOSITE OPERATIONAL AMPLIFIERS WITH A CMOS INTEGRATED CIRCUIT

by

Gary Steffen Kollmorgen

December 1986

Thesis Advisor: S. Michael

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Generation of Programmable Composite Operational Amplifiers with a CMOS Integrated Circuit

by

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Lieutenant, United States Navy
B.S., United States Naval Academy, 1977

Submitted in partial fulfillment of the
requirements for the degree of

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December 1986

ABSTRACT

A general approach for extending the useful operating frequencies of linear active networks is the Composite Operational Amplifier. The Composite Operational Amplifier is generated by replacing single operational amplifiers with a network of N operational amplifiers (CNOA). This novel approach is extended to the integrated circuit. Three, 2 operational amplifier (C2OA), composite forms are integrated on to a single chip. Additionally, the resistor network of the composite is constructed to be digitally programmable making the composite operational amplifiers capable of different Q factors. The chip is constructed with 200 transistors, four capacitors, and 10 resistors as major components. The overall size of the chip is 136 by 185 mils and is packaged in a 24 pin dual in-line package (DIP).

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I. INTRODUCTION

A. OPERATIONAL AMPLIFIERS

The Operational Amplifier (op-amp) is the most widely used analog integrated circuit. Prior to the development of integrated circuits, the op-amp was tolerable at best. With the increased dependence on integrated components in analog circuits, the op-amp has come to a level of importance unknown to a single component in past electrical history. With the growth of importance has also come the need for improved performance op-amps. Speed and accuracy are todays benchmarks. High speed analog-to-digital and digital-to-analog converters and high speed switched capacitor networks are at the forefront of technology.

Speed (slew rate) and accuracy (input offset voltage), as will be discussed below, are rarely achieved in a single op-amp design. Manufacturer's "high" accuracy CMOS and Bipolar op-amps (offset voltages on the order of 3 to 5 mV) are not sufficiently accurate for todays demanding applications. Bipolar op-amps with accuracies in the 100 microvolts range are available but have limiting slew rates (on the order of 10 Volts/μsec or less.) It was, until recently, nearly impossible to obtain a single op-amp that is both accurate and fast. Recent research has shown that, through a new design approach, high speed and accurate op-amps can be achieved. This technique is referred to as Composite Operational Amplifiers.

The general design procedure for Composite Operational Amplifiers is to combine N basic op-amps (e.g., LM741 or LF356) into a composite structure [Ref. 1]. The resulting op-amps were originally designed to meet or enhance several practical aspects of op-amp behavior. Among these aspects were stability, dynamic range, extended bandwidth (BW), supply voltage variations, gain bandwidth product (GBWP), and sensitivity. The composite op-amp technique will be discussed in detail (Chapter III) after the basic op-amp parameters and functionality are set forth below.

MOSFET analog operational amplifiers are a relatively new concept to the analog world previously dominated by the bipolar transistor operational amplifier. Bipolar design has been favored over MOS design in linear applications due to better transistor matching and higher transconductance (g_m) at similar operating levels [Ref. 2]. Today, many linear/digital systems are combined in MOS technology due to the advent of sampled data techniques. A brief comparison between bipolar and MOS technology will be covered in Chapter III.

It is essential that basic op-amp concepts be fully understood in order to understand and appreciate the benefits derived from the composite op-amp design. Chapter III will discuss the detailed background and theoretical aspects of the C2OAs, composites with two internal op-amps. Equations will be developed to show the transfer characteristics of the C2OAs. A historical background will also be presented on the development of CNOAs.

Chapter IV will develop the idea of placing C2OAs on a single integrated circuit. The bulk of the work done in this research will be described in Chapter IV. Actual CMOS op-amps will be examined through simulation and experimentation. These same op-amp designs will be placed on a single integrated chip using a chip designed at Ferranti Interdesign, Inc. called the Monochip. The resulting design will be sent to Ferranti Interdesign for digitization, further simulation and manufacture.

Chapter V will discuss the conclusions derived from the above experimentation and simulation. Extensions and improvements as well as areas for further research will also be put forth.

B. INPUT OFFSET VOLTAGE

An ideal op-amp that has both inputs connected to ground should create and output voltage (V_o) equal to zero (Figure 1.1). However, actual op-amps do not behave in this manner but rather exhibit a small DC voltage called the output offset voltage (V_{oo}). This voltage represents an error voltage and is undesirable in applications

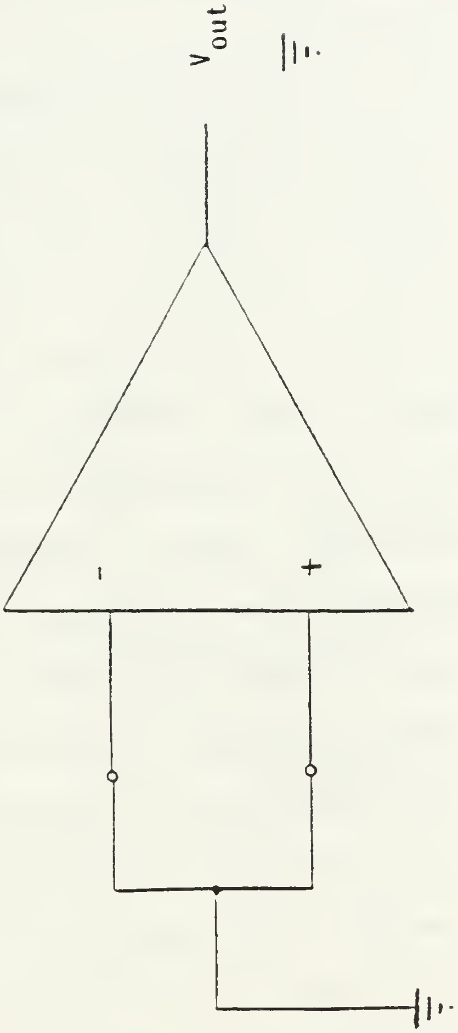


Figure 1.1 Offset Voltage

requiring high accuracy. The voltage required at the inputs in order to force the output to zero is referred to as the input offset voltage (V_{off}). The value of this voltage in most common operational amplifier is on the order of several millivolts.

V_{oo} is caused by a mismatching between the two op-amp input terminals. This mismatching, in bipolar op-amps, is caused by the transistor pairs in the input differential stage having different gains and internal resistances. These differences result in a non-zero differential first stage output voltage. This voltage is then amplified and even further corrupted by subsequent stages. Even in todays CMOS technology, where component design and tolerances is extremely high, component parameters still deviate about some statistical mean. As technology improves, input offset voltages decrease but are still a factor that needs consideration when using op-amps.

To reduce V_{oo} to zero an appropriate polarity and magnitude V_{off} must be applied to the op-amp. Unfortunately this voltage varies from op-amp to op-amp, even in the same type and lot. The correction must be applied from a compensating circuit capable of applying the correct voltage to null or balance the op-amp (Figure 1.2). This nulling network has limitations in that the offset voltage can vary with power supply deviations and operating temperature.

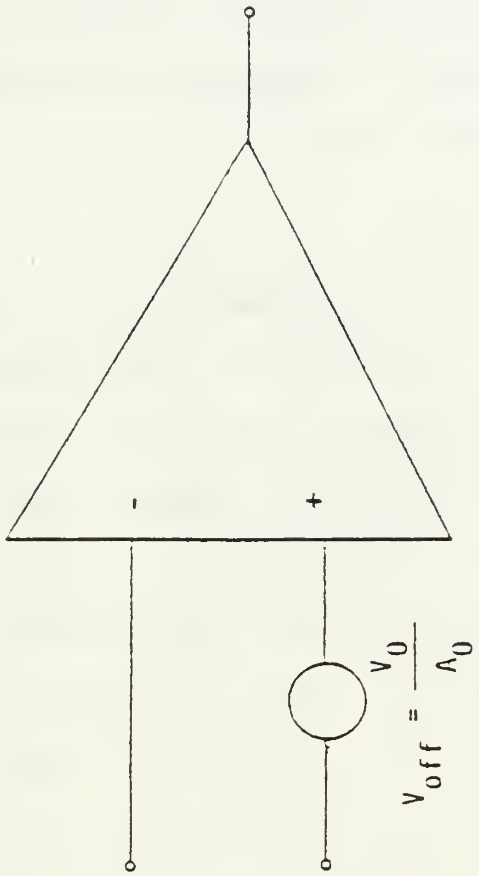


Figure 1.2 Offset Free Op-Amp

In a closed-loop configuration, the offset voltage will be multiplied by the gain of the circuit potentially creating a sizable error in the output signal. Because all op-amps have a limited dynamic range (slightly less than the supply voltages), an offset could severely limit the dynamic range of the input signal the op-amp could handle without the output being corrupted. Every op-amp will have an input offset voltage. Its acceptability depends on the application and accuracy desired.

C. SLEW RATE LIMITATIONS

Slew rate occurs in a non-small signal situation where the output signal is corrupted. This phenomenon is shown in Figure 1.3. The figure shows the difference in the slope of the input and output signals. Slew rate defines how rapidly the output voltage of an operational amplifier can change with respect to an instantaneous input voltage change. In mathematical terms, it is the maximum rate of output voltage change with respect to time assuming no signal distortion.

$$SR = \frac{dV_{out}}{dt} \quad \text{(maximized)} \qquad (1.1)$$

Slew rate is a problem associated with large signal inputs; that is signals with amplitudes comparable to the power supply voltages. Slew rate is generally measured in

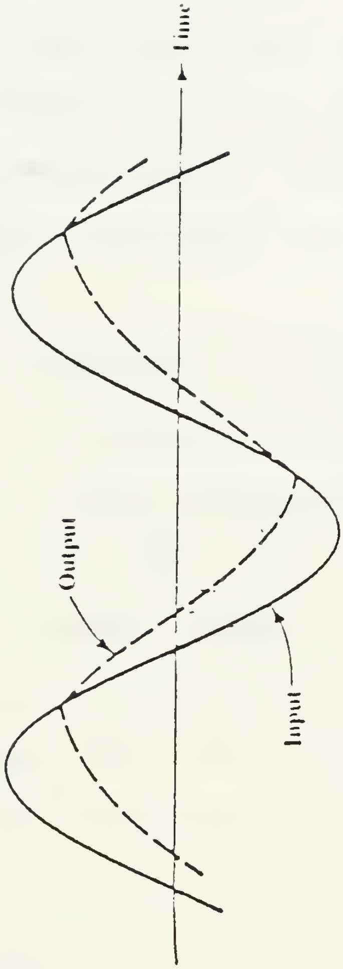


Figure 1.3 Illustration of Slew Rate Limiting

volts per microsecond. If an op-amp is specified to have a 1 volt per microsecond slew rate, it can be translated to mean that the output will change no faster than 1 volt every microsecond. In actuality, slew rate is not a constant in a given op-amp. It has been shown that slew rate is affected by the closed-loop gain, the DC supply voltages, and temperature. An increase in either closed-loop gain or DC supply voltage causes an increase in slew rate. An increase in temperature produces a decrease in slew rate [Ref. 3].

If in the circuit illustrated in Figure 1.4 an instantaneous step input voltage is applied, the output cannot respond instantaneously and is initially zero. This happens because the input stage (or input differential stage) transistors cannot handle the input voltage instantaneously and the internal capacitances will not be charged instantaneously. If the signal applied to the circuit of Figure 1.4 is a high frequency sinusoid then

$$V_{in} = V_{out} = V_p \sin \omega t \tag{1.2}$$

The rate of change with respect to time of the output is then

$$\frac{dV_{out}}{dt} = V_p \omega \cos \omega t \tag{1.3}$$

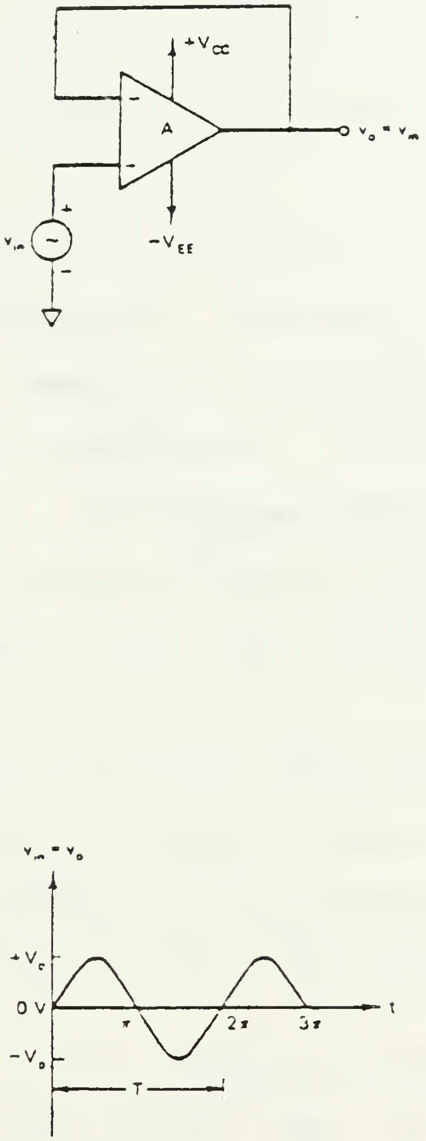


Figure 1.4 Voltage Follower for Slew Rate determination

The maximum change is when the COS term equals unity. Thus

$$SR = \frac{dV_{out}}{dt} (max) = V_p \ \omega \tag{1.4}$$

or

$$SR = \frac{2\pi f V_p}{10^6} \ (V/\mu s) \tag{1.5}$$

where f is the input frequency in hertz and V_p is the peak voltage of the input sine wave. This equation implies that the slew rate determines the maximum frequency for a distortion free output. If the peak voltage is set equal to the maximum voltage specified for the op-amp then the resulting frequency is denoted as the Full Power Bandwidth. This is the bandwidth over which linear operation is assured.

Slew rate limiting and the means to improve it in CMOS op-amps will be discussed in detail in Chapter II. It will be shown that MOSFET operational amplifiers inherently have better slew rates than their bipolar counterparts.

D. FREQUENCY DEPENDENT GAIN AND GBWP

A parameter of much concern when making use of operational amplifiers is the finite op-amp frequency dependent gain, A. Figure 1.5 shows a typical frequency response for an internally compensated bipolar op-amp.

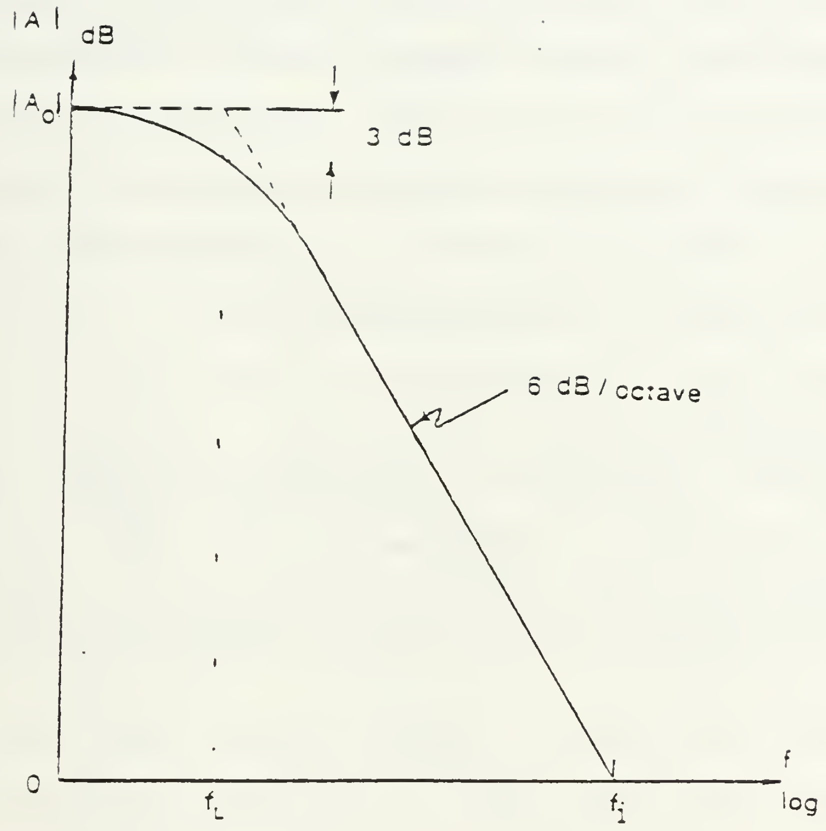


Figure 1.5 Typical Bipolar Operational Amplifier Frequency Response

Note the 3 dB frequency f_L (Hz), the unity gain frequency f_1 (Hz), and the uniform 20 dB per decade (6 dB per octave) roll-off caused by the internal compensating capacitor pole. Also of concern is the op-amp gain bandwidth product or GBWP. GBWP for a given op-amp is considered a constant. Equations defining frequency dependent gain and GBWP will be developed for CMOS op-amps in Chapter II. Bipolar op-amps have a GBWP of 10^5 to 10^7 hertz while a typical CMOS op-amp has a GBWP of 10^3 to 10^7 hertz. The dependency of an op-amp circuit's response to A and GBWP is of critical importance if an evaluation or comparison between op-amps is to have meaning.

E. CONCLUSIONS

The basic concepts of input offset voltage, slew rate limiting, frequency dependence, and GBWP have been discussed in general. In the next chapter, these factors will be looked at in detail as they apply to CMOS operational amplifiers. Chapter II will also show that an operational amplifier that is both fast (high slew rate) and accurate (low offset voltage) is impossible to obtain in a single op-amp. Chapter III will show how composites overcome the limitations of single operational amplifiers.

II. CMOS OPERATIONAL AMPLIFIERS

A. CMOS VERSUS BIPOLAR TRANSISTORS

The schematic representations of bipolar and MOSFET transistors are shown in Figure 2.1. For DC biasing there exists a direct correlation between the bipolar emitter, base, and collector and the MOSFET source, gate, and drain. This biasing relation is visualized in Figure 2.2. A significant difference is at the base/gate node of the respective transistors. A bipolar transistor is current controlled by I_b whereas the MOSFET is voltage controlled by V_{GS}. In both types of transistors, transconductance (g_m) is a parameter of interest. Therefore, V_{BE} and V_{GS} are the controlling functions for their respective transistors. The output current and transconductance equations for the bipolar transistor are respectively

$$I_C = I_S \{\exp[qV_{BE}/(nKT)] -1\} \tag{2.1}$$

$$g_m = I_C q/(nKT) \tag{2.2}$$

The equations for the MOSFET transistor are respectively

$$I_{DS} = K(V_{GS} - V_T)^2 \tag{2.3}$$

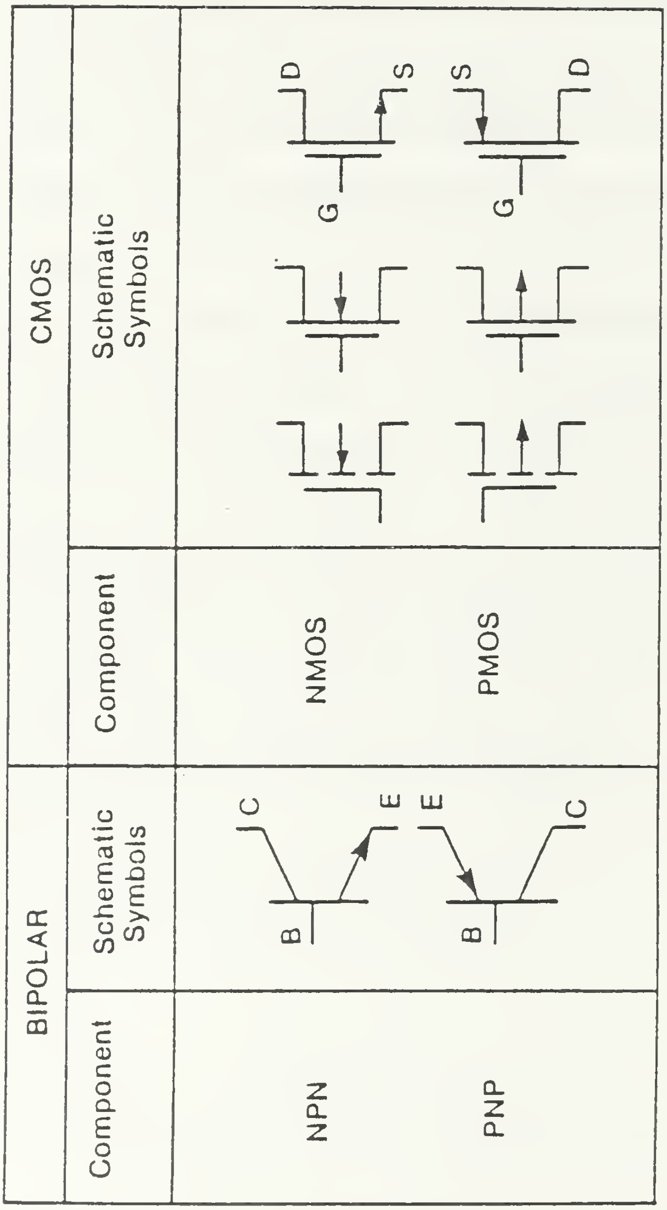


Figure 2.1 Schematic Symbols for Bipolar and Corresponding MOS Transistors

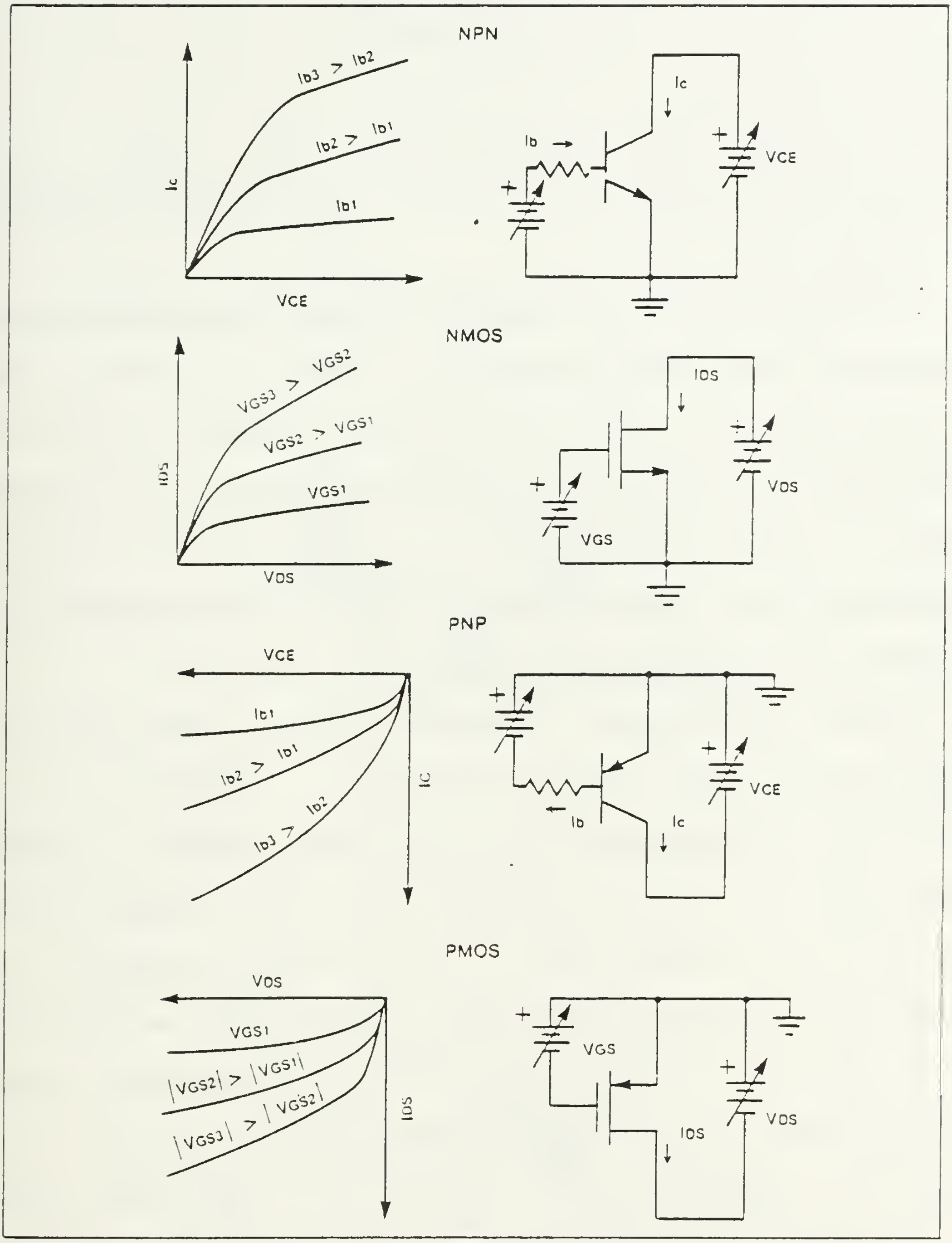


Figure 2.2 DC Output Characteristic Comparisons for Bipolar and Corresponding MOS Transistors

$$g_m = 2(KI_{DS})^{1/2} \tag{2.4}$$

It is important to note that I_C in the bipolar is an exponential function of V_{BE} but I_{DS} is a square function of V_{GS}. [Ref. 2]

Unlike the bipolar transistor which, regardless of the transistors size, has a typical g_m equal to 40,000 micromho at 1mA of operating current, the g_m of a MOSFET is directly proportional to the square root of the ratio of its channel width to length. Therefore K in Equation 2.3 must be calculated from given process parameters (surface mobility and gate oxide capacitance/unit area) [Ref. 2].

The MOS and bipolar transistors have other pertinent comparisons. The turn-on threshold voltage (V_T) of a MOSFET can be compared to V_{BE} of the bipolar. Typical values are 1 volt for the MOSFET threshold voltage and 0.6 volts for the bipolar V_{BE}. The operating regions of the MOSFET and the bipolar transistor are reversed as in Figure 2.3. The linear region for the bipolar transistor, where it is used as a linear amplifier, is where I_C is essentially constant for a given V_{BC}. The linear region for a MOSFET is where V_{DS} is very small and the device acts as a voltage controlled variable resistor. The MOSFET is used as a linear amplifier when its operated in its

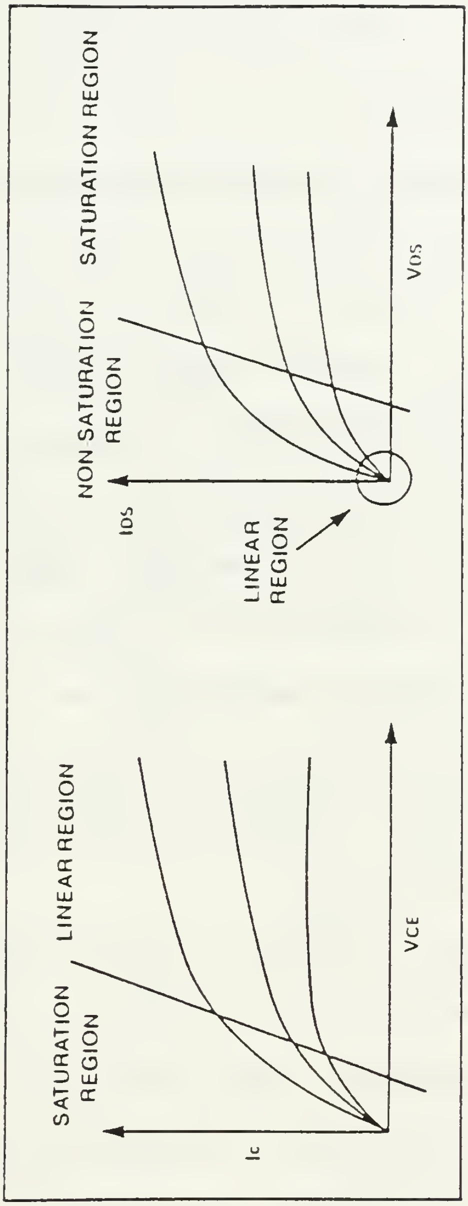


Figure 2.3 Operating Regions for Bipolar and MOS Transistors

saturated region. Finally, the switching speed of the bipolar is severely degraded if V_{CE} drops into the saturation region. The MOSFET, being a unipolar device, simply looks resistive if V_{DS} drops to zero volts and loses very little switching speed. [Ref. 2]

B. INPUT OFFSET VOLTAGE

Input offset voltage was discussed and defined in Chapter I. The major factors that affect the input offset voltage of a CMOS op-amp are the width to length ratio (W/L) of the input stage transistors, differences in individual transistor threshold voltages, and the W/L of the current mirror (Figure 2.4) in the first stage. The W/L ratio of the input differential pair transistors and the current mirror transistors of Figure 2.4 contribute to what is called systematic offset while the differences in the ideally symmetric transistors due to fabrication is called random offset. Each of the factors will be individually discussed below.

The effect of the width to length (W/L) ratio of the input stage transistors is minimized as the W/L of the transistors is increased. Increasing the width reduces mismatch caused by diffusion irregularities at the two sides of the channel of the transistors. Increasing L reduces the mismatch due to diffusion irregularities in the source-drain diffusion lateral profile [Ref. 4].

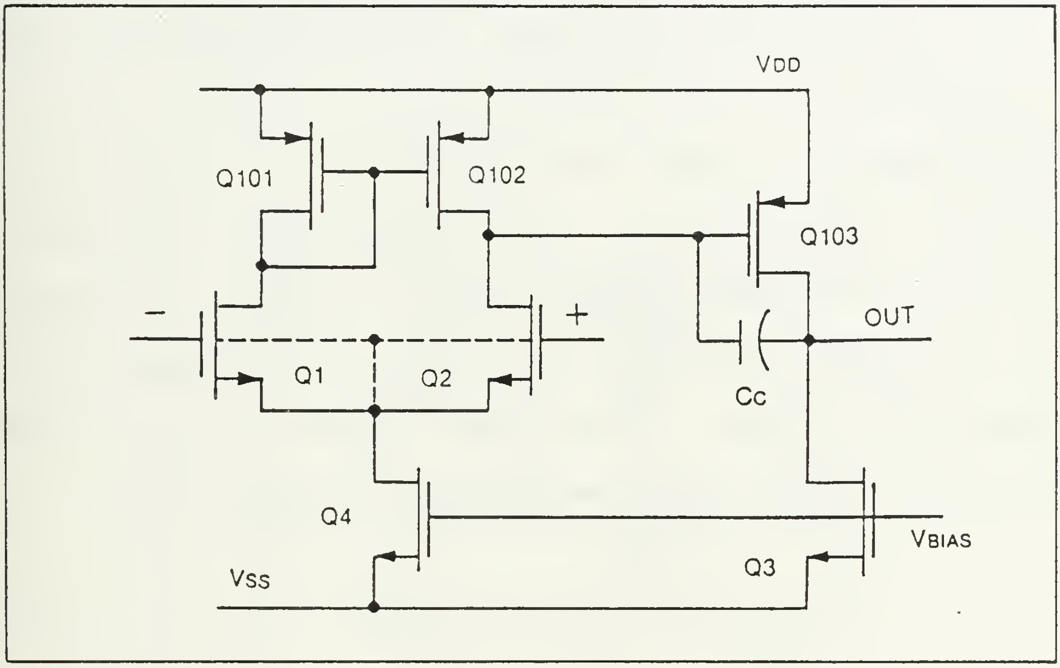


Figure 2.4 Basic CMOS Operational Amplifier

Due to local diffusion variations, there will be differences in the threshold voltages of the individual transistors. This will contribute directly to mismatching between the input stage transistors and input offset voltage. If the transistors are "quaded" or paralleled as in Figure 2.5, the affect of diffusion variations and thus threshold voltages will be canceled.

In a properly designed CMOS operational amplifier only the transistors in the first stage contribute to V_{OFF}. This includes the input differential pair transistors and the active current mirror load. The input differential pair transistors contribute directly to V_{OFF}. This means that a mismatch in these transistors of 1mV appears as a 1mv amplifier offset. The active current mirror loads contribute to total offset according to Equation 2.5.

$$V_{off} = (g_{mi}/g_{ml})\ V_{off-load} \qquad (2.5)$$

Where g_{mi} is the transconductance of the differential pair transistors, g_{ml} is the transconductance of the current mirror transistors, and $V_{off-load}$ is the offset voltage of the current mirror load [Ref. 2].

The operational amplifier layouts used in this analysis use equal numbers of complimentary transistors for the differential pair and the current mirror load. Therefore, using Equation 2.5 the current mirror contributes directly

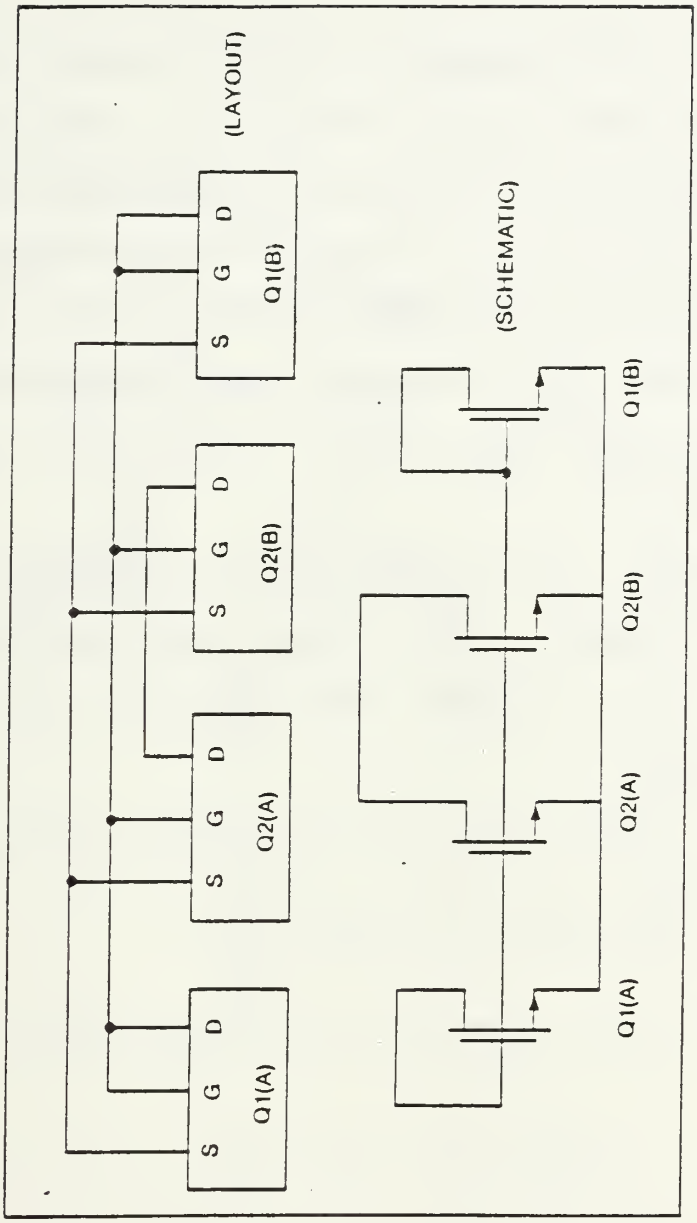


Figure 2.5 Quaded Transistors Current Mirror

to the amplifier offset. That is, a 1mV mismatch between the current mirror transistors contributes 1mV to V_{off}. [Ref. 2]

The effect of systematic offset can be illustrated using the two-stage op-amp in Figure 2.6. The differential stage is composed of Q1 through Q5 while the single ended gain stage is Q6 and Q7. If there is no systematic offset, then grounding the input terminals will yield a zero output voltage. If the output terminal is now grounded the output current, I_{out}, must equal zero. This leads to I_6 and I_7 equal to zero.

Assuming that the transistors have symmetric geometry, then $(W/L)_1$, $(W/L)_2$, $(W/L)_3$, and $(W/L)_4$ are equal. This implies that the currents and voltages will also be symmetric. Thus,

$$V_{DS3} = V_{DS4} \text{ and } V_{GS3} = V_{GS6} \qquad (2.6, 2.7)$$

If the value of V_{GS6} results in I_6 being equal to I_7 when

$$V_{DS6} = 0 - V_{DD} = -V_{DD} \qquad (2.8)$$

then

$$I_{out} = 0 \qquad (2.9)$$

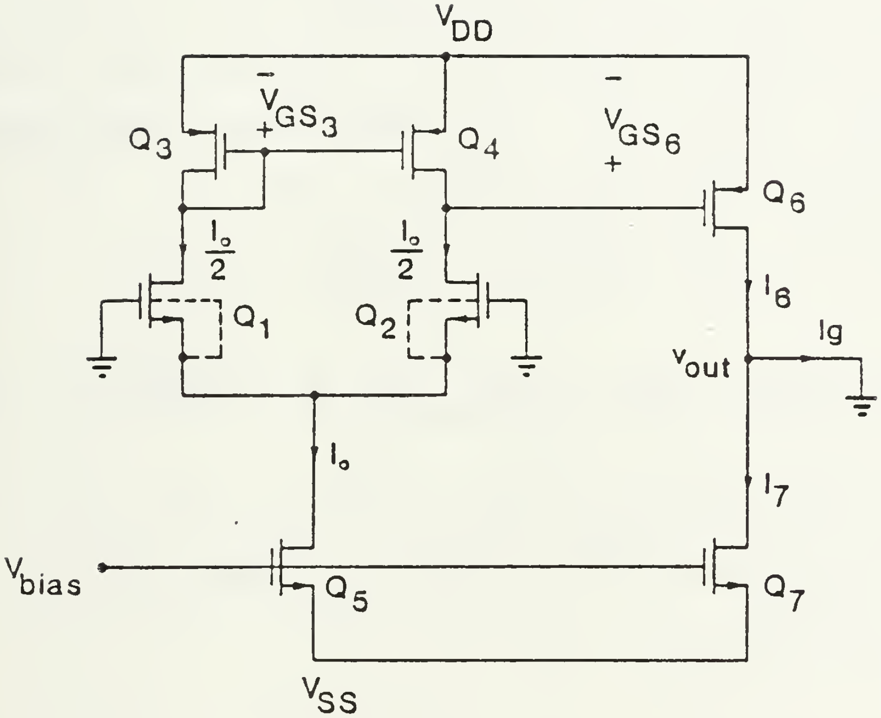


Figure 2.6 Two-stage CMOS Op-amp

as required. If this is not the case, and I_{out} does not equal zero, a systematic offset exists. [Ref. 4]

Let V_{GS6}' denote the value of V_{GS6} necessary to make I_6 equal to I_7. The input offset voltage is

$$V_{off} = \frac{(V_{GS6} - V_{GS6}')}{A_d} = \frac{(V_{GS3} - V_{GS6}')}{A_d} \qquad (2.10)$$

where A_d is the voltage gain of the input stage. Assuming that all devices are in saturation and neglecting modulation effects, the voltages of Q3 and Q4 can be expressed as

$$V_{GS3} = V_{DS3} = V_{GS4} = V_{DS4} = V_{TP} + \sqrt{\frac{(I_o/2)}{K_p(W/L)_3}} \qquad (2.11)$$

V_{TP} is the threshold voltage of Q3 and Q4 and kp is the constant transconductance factor for PMOS devices. The voltage for Q6 is,

$$V_{GS6} = V_{TP} + \sqrt{\frac{I_6}{K_p(W/L)_6}} \qquad (2.12)$$

Substitute $V_{GS6} = V_{GS3}$ and $I_6 = I_7$ into Equation 2.12

$$V_{GS3} = V_{TP} + \sqrt{\frac{I_7}{K_p(W/L)_6}} \qquad (2.13)$$

From Equation 2.11 and 2.13 the condition,

$$\frac{(W/L)_3}{(W/L)_6} = \frac{I_o/2}{I_7} \qquad (2.14)$$

is necessary for zero offset. Looking at Q5 and Q7, since their gate-to-source voltages are equal and neglecting channel length modulation,

$$\frac{(W/L)_5}{(W/L)_7} = \frac{I_o}{I_7} \qquad (2.15)$$

Combining equations 2.14 and 2.15

$$\frac{(W/L)_3}{(W/L)_6} = \frac{(W/L)_4}{(W/L)_6} = \frac{1}{2}\ \frac{(W/L)_5}{(W/L)_7} = \frac{I_o}{2I_7} \qquad (2.16)$$

If Equation 2.16 is satisfied then the currents I_6 and I_7 are equal and V_{out} equal to zero is possible. If the gate to source voltages are not compatible and the output terminal is open-circuited, then V_{out} is non-zero. The drain voltages of Q6 and Q7 will compensate for the incompatibilities in the gate voltages. This may result in the transistors operating out of saturation. This will represent a major systematic offset and can significantly reduce the gain and bandwidth of the op-amp.

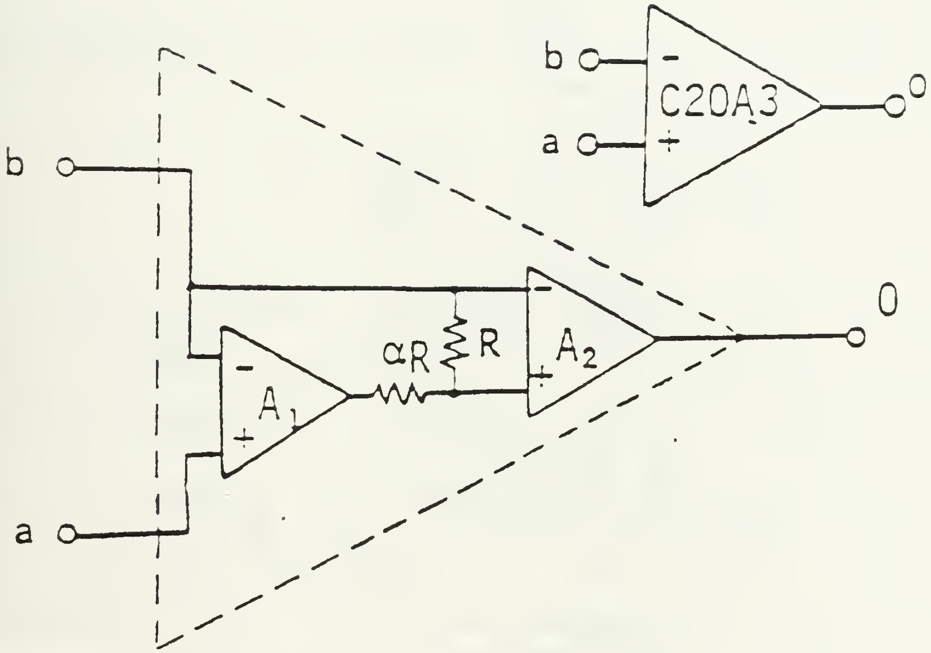
Typical values for CMOS operational amplifier input offset voltages are 5-15 mV. Chapter IV will list the values found in the CMOS op-amps used in this study. It will also be shown that the composite op-amp will yield an overall input offset voltage approximately equal to the offset voltage of the op-amp placed in the A1 or input position (Figure 2.7).

C. SLEW RATE LIMITATIONS

Slew rate is a large signal phenomenon as discussed in Chapter I. For a large input step voltage, some of the transistors in the op-amp may be driven out of their saturation (linear) region or completely cut off. As a result the output is not capable of following the input at the same rate. This slewing is not directly related to the frequency response. Typical values for CMOS op-amp slew rates are 1 to 20 volts per microsecond. The slew rate is dependent on the bias current and the compensation capacitor.

Figure 2.8 is used as the large signal model in evaluating slew rate. Before the input step voltage is applied the currents in Q1 and Q2 are both equal ($I_o/2$). After the arrival of the large step, Q1 conducts more current and cuts off Q2. Thus the current in Q1 and Q3 is equal to I_o. Because Q3 and Q4 form a current mirror, the current in Q4 is also I_o. Assuming the output stage, A2 can sink the current, I_o, the slew rate is

$$SR = \left|\frac{dV_{out}}{dt}\right| = \left|-\frac{1}{C_c}\frac{dQ_c}{dt}\right| = \frac{I_o}{C_c} \qquad (2.17)$$



C20A-3 .

Figure 2.7 Composite Operational Amplifier Showing Input[A1] and Output[A2] Positions

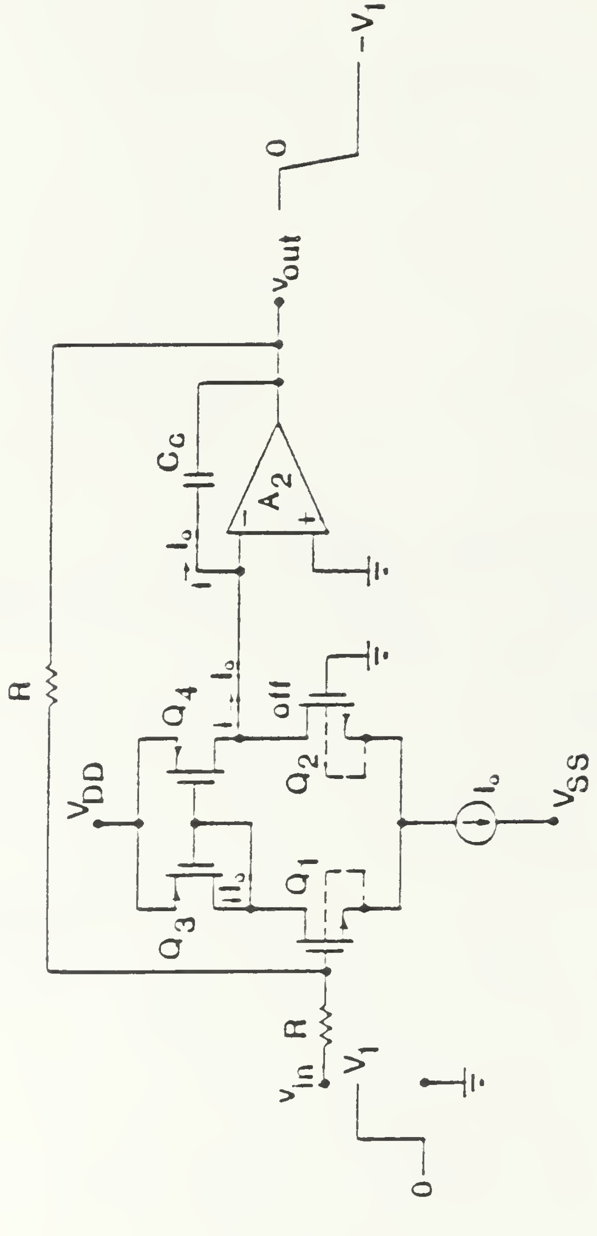


Figure 2.8 Large Signal Model for Calculating Slew Rate of CMOS Op-amp

where Q_c is the charge in C_c. C_c in turn is

$$C_c = g_{mi}/\omega_o \tag{2.18}$$

where ω_o is the unity-gain frequency and

$$g_{mi} = 2\sqrt{\frac{I_o}{2} K' \frac{W}{L}} \tag{2.19}$$

Combining Equations 2.18 and 2.19 with 2.17 yields

$$SR = \frac{I_o \omega_o}{g_{mi}} = \omega_o \sqrt{\frac{I_o}{2K' W/L}} \tag{2.20}$$

It can be easily seen from Equation 2.20 that the slew rate of a CMOS op-amp can be increased by increasing the unity-gain bandwidth of the input stage[Ref. 4]. This method is used in most high slew rate circuits. The frequency characteristics of the transistors in the integrated circuit limit the maximum unity-gain bandwidth. The other method to increase slew rate is to decrease the ratio of the first stage transconductance (g_m) to bias current. This is achieved by using MOSFET transistors with low g_m inherent in a CMOS op-amp. This explains the slew rate improvement in CMOS op-amps over their bipolar counterparts. The limitation to this method is increased offset voltage inherent in the MOSFET circuit. MOSFETs are known to have higher input offset voltages than do bipolar transistors, by at least a factor of 3 and often much more [Ref. 5].

In bipolar op-amps a method used to decrease the g_m to operating current ratio is by including emitter-degeneration resistors in the input differential amplifier. Again the penalty is paid in an increased offset voltage and drift if the resistors do not match extremely well. Other methods used to increase slew rate have been successful but as before there is a corresponding increase in offset voltage [Ref. 5].

D. FREQUENCY DEPENDENT GAIN AND GBWP

Figure 2.9 shows the DC gain, A_o, the uniform 20 dB per decade roll-off, and the poles and zeros of a typical CMOS op-amp frequency response. S_{P1} is the frequency of the first pole in the associated gain or transfer function. It is affected primarily by the internal compensating capacitor of the op-amp. S_{P2} is the second pole frequency of thee transfer function and is a result of the compensation capacitor and the internal parasitic capacitances. S_{Z1} is the zero of the transfer function and has its roots in the transconductances of the output stage transistors. The work done in this thesis assumes that all of the op-amps being studied will be stable and show this type of frequency response. The gain equation, if the op-amp is compensated, can be approximated by

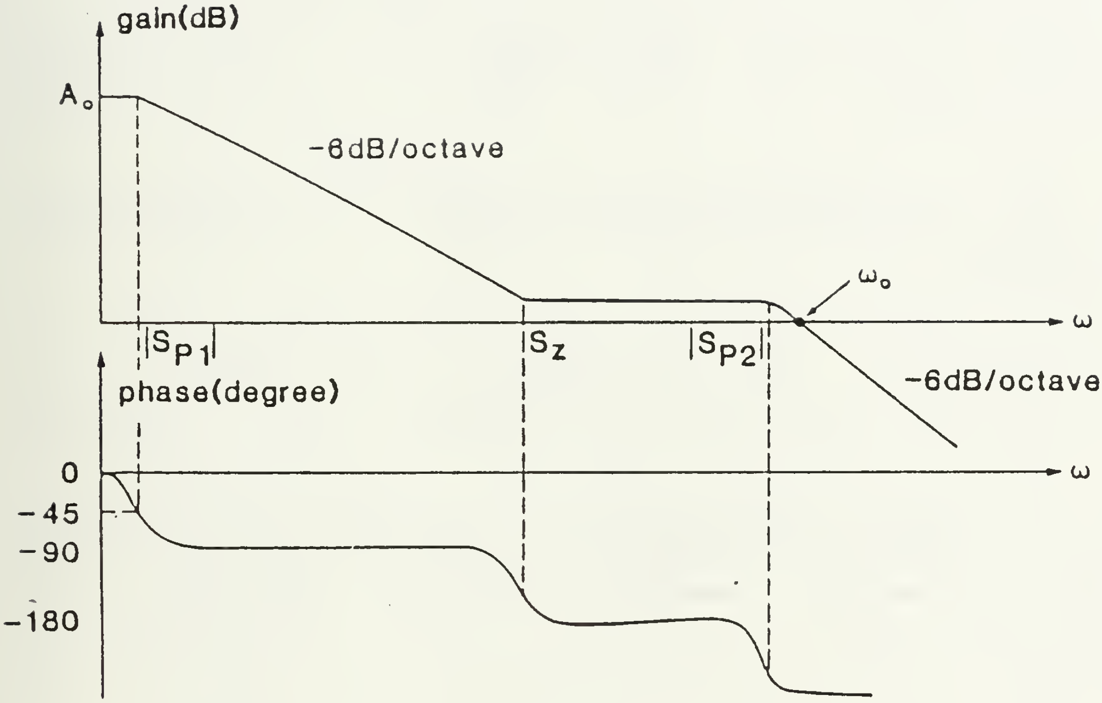


Figure 2.9 Typical Frequency Response of the CMOS Op-amp

$$A(s) = \frac{A_o}{1 + (s/s_{p1})} \qquad (2.21)$$

Where A_o is the DC gain value and S_{P1} is measured in radians per second. For frequencies much greater than SP1, this expression becomes

$$A(s) = \frac{A_o s_{p1}}{s} \qquad (2.22)$$

Thus the Gain Bandwidth Product (GBWP), ω_i, of the op-amp is given by

$$\omega_i = A_o s_{p1} \qquad (2.23)$$

which is generally considered as a constant and is used as a figure of merit. Combining Equations 2.22 and 2.23 yields

$$A(s) = \omega_i/s \qquad (2.24)$$

or

$$\left|A(s)\right| = \omega_i/\ \omega \qquad (2.25)$$

Both A_o and f_i (ω_i, expressed in hertz) are temperature and power supply dependent. As stated in Chapter I, typical values for the GBWP of a CMOS op-amp are 10^3 to 10^7.

E. CONCLUSIONS

This chapter elaborated on the points made in Chapter I as they apply to CMOS operational amplifiers. There are many similarities between bipolar and MOSFET op-amps. However, the differences are of significance. The low transconductance of the MOS transistor affects both the slew rate (improving it) and the offset voltage (degrading it). Through various techniques these differences are minimized. For purposes of this study the differences are considered negligible. The CMOS op-amp will be tested and used in the same manner as it bipolar counterpart.

Additionally, several methods to increase slew rate were put forth. The increase in slew rate in all cases had a corresponding increase in offset voltage. The composite operational amplifier discussed in Chapter III will show means of achieving both high slew rate and low offset in a "single" op-amp.

III. COMPOSITE OPERATIONAL AMPLIFIERS

A. GENERATION OF CNOA'S

Composite Operational Amplifiers were developed by S.N. Michael and W.B. Mikhael in 1980. Investigations into their behavior has been discussed in the literature [Refs. 1,6-9]. The initial studies were trying to develop a technique of increasing useful bandwidth (BW) of circuits using operational amplifiers. Active compensation was examined and applied to the design of active filter networks. The resulting composite devices have three external terminals that resemble those of a standard op-amp.

A complete study was made using basic operational amplifiers in numerous configurations to determine which configurations would yield amplifiers with both amplitude and phase compensation. Nullator-norator pairing was used to yield 136 possible circuit networks. These networks were then further examined according to the following criteria:

1. Let $A_a(s)$ and $A_b(s)$ be the non-inverting and inverting open loop gains of each of the 136 C2OA's examined. The denominator polynomial coefficients of $A_a(s)$ and $A_b(s)$ should have no change in sign. This satisfies the necessary (but not sufficient) conditions for stability. Also, none of the numerator or denominator coefficients of $A_a(s)$ and $A_b(s)$ should be realized through differences. This eliminates the need for single op-amps of matched

GBWPs and results in low sensitivity of the C2OA with respect to its components.

2. The external three terminal performance of the C2OAs should resemble, as close as possible, from the versatility point of view those of the single op-amp.

3. No right half S plane (RHS) zeros due to the single op-amp pole should be allowed in the closed loop gains of the C2OAs (for minimum phase shifts).

4. The resulting input-output relationship $T_a(s)$ in the applications considered should have extended frequency operation with minimum gain and phase deviation from the ideal transfer function $T_i(s)$. The improvement should be enough to justify the increased number of op-amps.

Only twenty seven of the 136 composite networks were found to have acceptable performance. From these twenty seven, four were found to have superior performance over the other C2OAs. These structures are shown in Figures 3.1 through 3.4.

The same techniques and basic approach were used for CNOAs where $N > 2$. Figure 3.5 shows the designs yielded for $N = 3$. In all cases the performance was improved as the number of active elements was increased. For this study only C2OAs will be used although the designs generated here can be expanded to include CNOAs where $N>2$.

It was shown in Ref. 1 that the open-loop gain input-output relationships are given by those shown in Figure 3.6. The transfer functions, 3 dB frequency equations, and Q equations for C2OAs are shown in Figure 3.7. These two figures are the mathematical background necessary for the

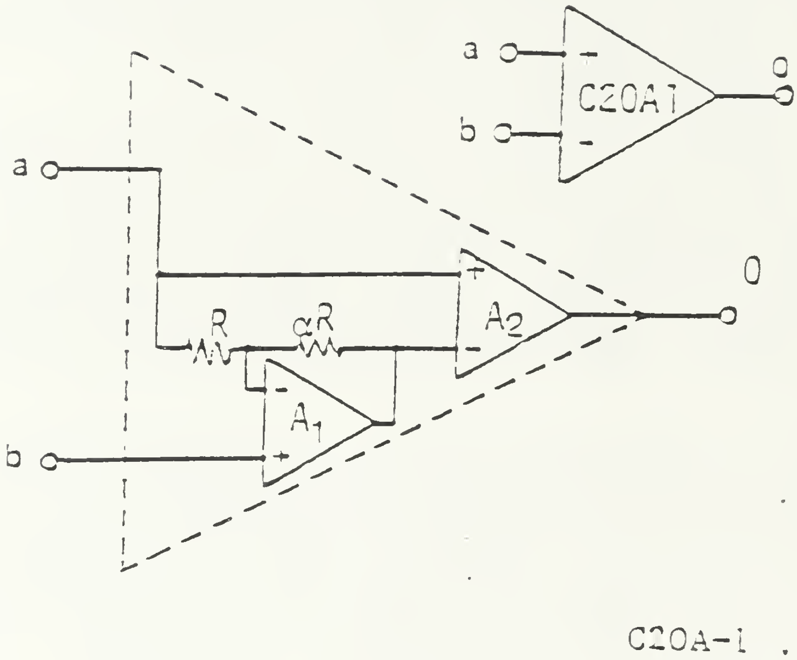
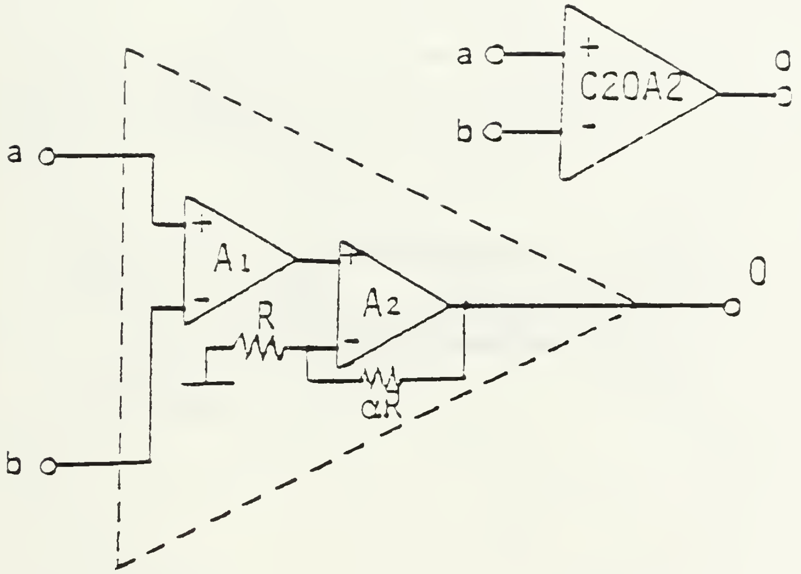


Figure 3.1 C20A-1 Operational Amplifier



C20A-2 .

Figure 3.2 C20A-2 Operational Amplifier

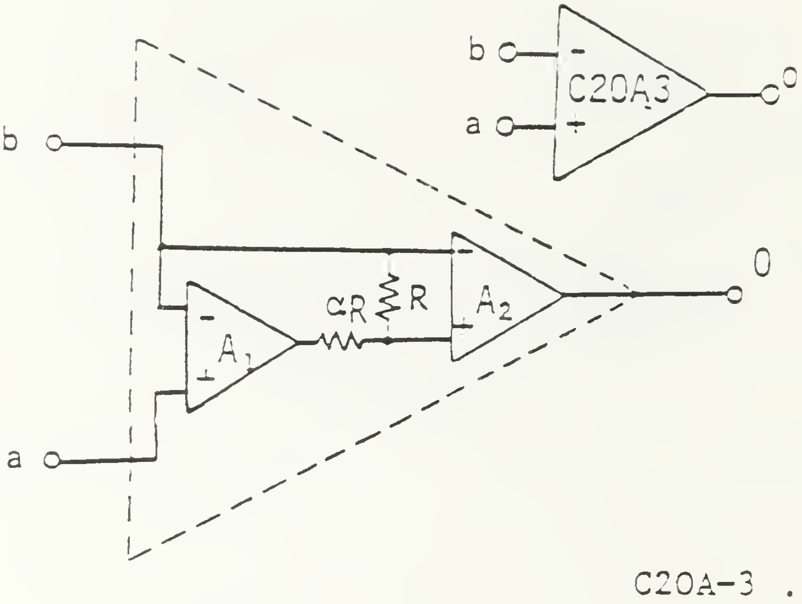
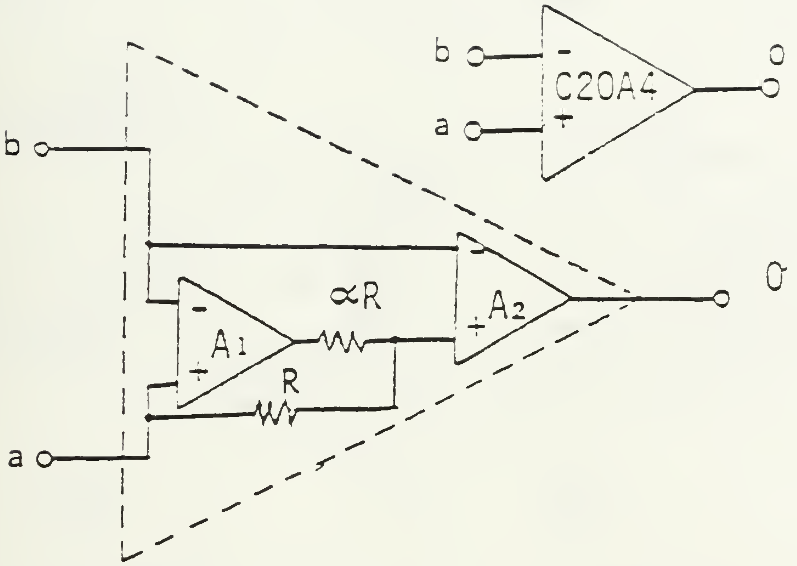


Figure 3.3 C20A-3 Operational Amplifier



C20A-4 .

Figure 3.4 C20A-4 Operational Amplifier

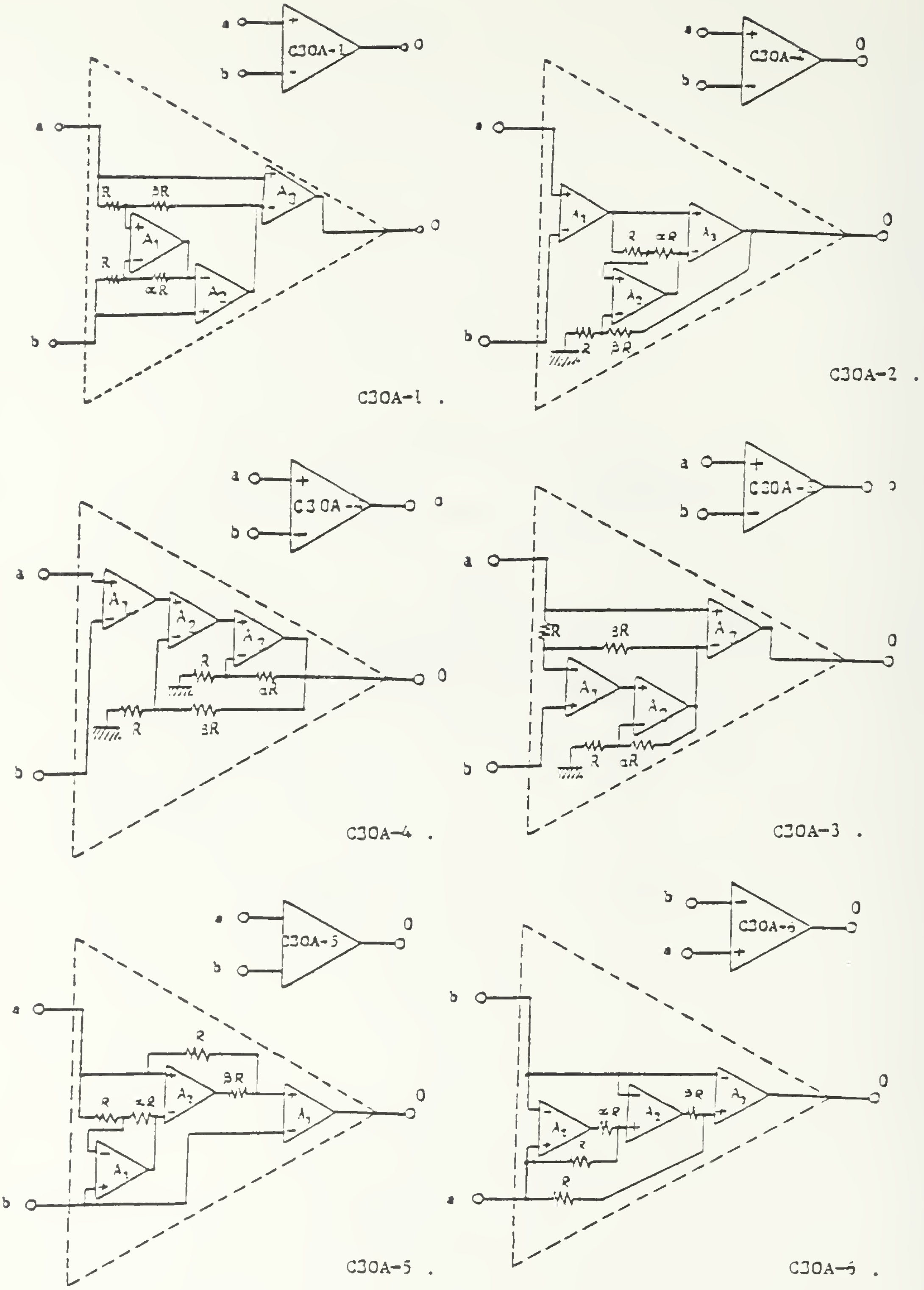


Figure 3.5 C30A Composite Operation Amplifiers

$$V_{0i} = V_a A_{ai}(s) - V_b A_{bi}(s) \qquad (i = 1 \text{ to } 4)$$

for C20A-1:

$$V_{01} = V_a \frac{A_2 (1 + A_1) (1 + \alpha)}{A_1 + (1 + \alpha)} - V_b \frac{A_1 A_2 (1 + \alpha)}{A_1 + (1 + \alpha)}$$

for C20A-2:

$$V_{02} = V_a \frac{A_1 A_2 (1 + \alpha)}{A_2 + (1 + \alpha)} - V_b \frac{A_1 A_2 (1 + \alpha)}{A_2 + (1 + \alpha)}$$

for C20A-3:

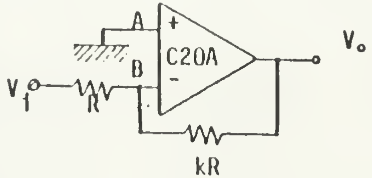
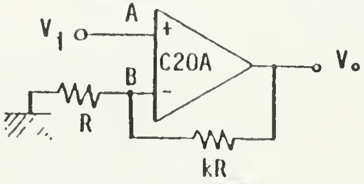
$$V_{03} = V_a \frac{A_1 A_2}{(1 + \alpha)} - V_b \frac{A_2 (1 + A_1)}{(1 + \alpha)}$$

for C20A-4:

$$V_{04} = V_a \frac{A_2 (A_1 + \alpha)}{(1 + \alpha)} - V_b \frac{A_2 \{ A_1 + (1 + \alpha) \}}{(1 + \alpha)}$$

where α is the internal resistor ratio

Figure 3.6 C20A Open-loop Gain Input-Output Relationships

C20A·	Negative Finite Gain Trans. Function (Ta)	Positive Finite Gain Trans. Function (Ta)	ω_p	Q_p
C20A-1	$T_1 \dfrac{1}{1 + (S/\omega_p Q_p) + (S^2/\omega_p^2)}$	$T_1 \dfrac{(1+S/\omega_1)}{1 + (S/\omega_p Q_p) + (S^2/\omega_p^2)}$	$\sqrt{\dfrac{\omega_1\omega_2}{1+k}}$	$\dfrac{(1+\alpha)}{\sqrt{1+k}}\sqrt{\dfrac{\omega_2}{\omega_1}}$
C20A-2	$T_1 \dfrac{1}{1 + (S/\omega_p Q_p) + (S^2/\omega_p^2)}$	$T_1 \dfrac{1}{1 + (S/\omega_p Q_p) + (S^2/\omega_p^2)}$	$\sqrt{\dfrac{\omega_1\omega_2}{1+k}}$	$\dfrac{(1+\alpha)}{\sqrt{1+k}}\sqrt{\dfrac{\omega_1}{\omega_2}}$
* C20A-3	$T_1 \dfrac{(1+S/\omega_1)}{1 + (S/\omega_p Q_p) + (S^2/\omega_p^2)}$	$T_1 \dfrac{1}{1 + (S/\omega_p Q_p) + (S^2/\omega_p^2)}$	$\sqrt{\dfrac{\omega_1\omega_2}{(1+k)(1+\alpha)}}$	$\sqrt{\dfrac{(1+k)(1+\alpha).\omega_1}{\omega_2}}$
C20A-4	$T_1 \dfrac{[1+(1+\alpha)S/\omega_1]}{1 + (S/\omega_p Q_p) + (S^2/\omega_p^2)}$	$T_1 \dfrac{(1+\alpha S/\omega_1)}{1 + (S/\omega_p Q_p) + (S^2/\omega_p^2)}$	$\sqrt{\dfrac{\omega_1\omega_2}{(1+k)(1+\alpha)}}$	$\sqrt{\dfrac{(1+k)}{(1+\alpha)}\cdot\dfrac{\omega_1}{\omega_2}}$
				
	$\dfrac{V_o}{V_1} = - k = T_1$	$\dfrac{V_o}{V_1} = (1+k) = T_1$	T_1(ideal Transfer Function)	

* $\alpha R_1 \ll kR$ (for maximum ω_p)

Figure 3.7 C20A Finite Gain Transfer, 3 dB Point (ω_p), and Qp Functions

study of C2OAs in this thesis. It should be noted that Q and the 3 dB frequency equations are a function of the compensation resistor ratio α and the closed loop gain K. It would be desirable in most applications to select the suitable α and K that would yield an acceptable amplitude and phase deviation of the actual transfer function from the ideal and still satisfy any requisite conditions for stability. Via the Routh-Hurwitz stability criterion, the necessary and sufficient conditions for stability can be shown to be:

$$1 + \alpha < \frac{1+K}{2} \tag{3.1}$$

for C2OA-1 and C2OA-2 and

$$1 + \alpha > 1+K \tag{3.2}$$

for C2OA-3 and finally

$$1 + \alpha > 4(1+K) \tag{3.3}$$

for C2OA-4.

B. INPUT OFFSET VOLTAGE

Input offset voltage, as stated earlier, is a significant performance factor for an op-amp. It places a lower limit on the DC voltage that can be accurately detected and amplified. No two op-amps can produce in exactly the same manner, which includes offset voltage. Because of this, input offset voltage must be treated as a random variable. This randomness holds for both bipolar and MOS op-amps.

Because the distribution of the random parameter can only be generalized with many assumptions, an exact determination of the offset voltage from the transistor level is unlikely if not impossible. However, an attempt to predict the input offset of the composite op-amp based on the "known" offsets of the internal op-amps was made. This approach to determining offset was not difficult and will be covered below for the case of C20A-3.

Using the circuit shown in Figure 3.8, Equation 3.4 and 3.5 may be written as

$$V_1 = A1\ V_3 \tag{3.4}$$

and

$$\frac{(V_2 - V_1)}{\alpha R} = \frac{(V_3 - V_2)}{R} \tag{3.5}$$

Putting 3.4 into 3.5 gives

$$V_2 - A1\ V_3 = \alpha V_3 - \alpha V_2 \tag{3.6}$$

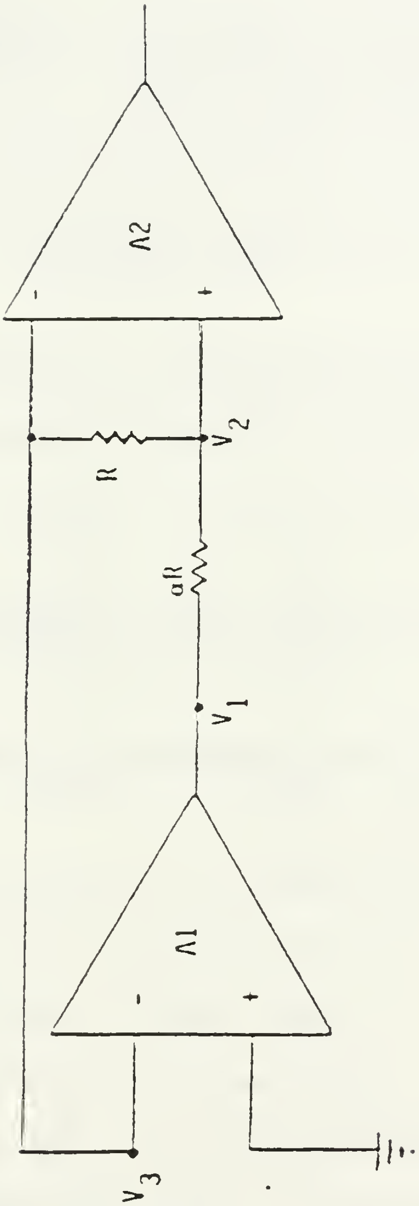


Figure 3.8 Circuit for Determining the Input Offset Voltage for the C20A-3

rearranging 3.6

$$V_3 = V_2 \frac{(1 + \alpha)}{(A1 + \alpha)} \tag{3.7}$$

If V_{off2}, the voltage required to offset op-amp A2, is reflected back to the input, then

$$V_3 = V_{off2} \frac{(1 + \alpha)}{(A1 + \alpha)} \tag{3.8}$$

Since the voltage required to offset op-amp A1 is V_{off1}, the input offset voltage for the composite, V_{off} may be written as

$$V_{off} = V_{off1} + [V_{off2} \frac{(1 + \alpha)}{(A1 + \alpha)}] \tag{3.9}$$

where the term (A1 + α) can be approximated by A1 since A1 is much larger than α.

Using similar techniques, the input offset voltages for the other composites can be shown to be those listed in Figure 3.9. In every case, except C20A-1, it is interesting to note that the portion of offset due to A2 is divided by the open-loop gain of the A1 op-amp. Because the open-loop gain of A1 is many magnitudes larger than the offset of A2, the total offset can be considered to be that of A1 only. This simplification can be applied to C20A-1 also given α large.

C20A-1 $V_{off} = V_{off1} + (V_{off2} / \alpha)$

C20A-2 $V_{off} = V_{off1} + (V_{off2} / A1)$

C20A-3 $V_{off} = V_{off1} + \{ V_{off2} (1 + \alpha) / A1 \}$

C20A-4 $V_{off} = V_{off1} + \{ V_{off2} (1 + \alpha) / A1 \}$

Figure 3.9 C20A Input Offset Voltages

The importance of the equations in Figure 3.9 is that a very accurate composite (low V_{off}) can be generated using an op-amp with with a small input offset voltage in the A1 position. The A2 position op-amps input offset voltage is for most purposes negligible.

C. SIGNIFICANCE OF COMPOSITE AMPLIFIERS

It was shown in Chapter II that through relatively simple means the slew rate of a CMOS amplifier can be improved. But, as in the case of the bipolar op-amp, as slew rate is improved the offset voltage deteriorates to unacceptable levels. Studies indicated, since composite operational amplifiers are tolerant of mismatched individual op-amp GBWPs, that CNOAs might provide a unique capability to be designed to meet certain specifications. This could be achieved by selecting op-amps with different performance characteristics and by varying α to meet the desired requirements.

The equations of Figure 3.9 indicate that the use of a precision op-amp, one with little DC error or offset, in the A1 position of the C2OAs would provide excellent front-end characteristics and control the offset voltage of the composite. Additionally, a high slew rate, fast settling, and wide bandwidth op-amp in the A2 position, would provide a fast output stage and, in turn, a fast composite.

The slew rate and bandwidth limitations of the front-end, or A1 op-amp, will have little effect on the output of the composite. It can be easily shown that the output of the A1 op-amp, which is an internal node in each of the C2OAs, will always be much less than the output voltage swing. Therefore, no distortion or dynamic range limitations due to the limited performance of the front-end should be seen in the output of the composite. The C2OA should show all the output performance characteristics of the A2 op-amp.

D. CONCLUSIONS

The concept of composite operational amplifiers and the general approach to their generation was presented. The potential for developing high speed, high accuracy, operational amplifiers that extend the useful operating frequencies of linear active networks, was discussed. Of the 136 different C2OA combinations achievable through this technique, four were shown to satisfy the given criteria and deliver superior performance.

The C2OAs were analyzed for input offset voltage. It was exhibited that the input offset of the composite op-amp will be approximately the same as the op-amp occupying the A1 position.

While the A1 position determines the accuracy or offset of the composite, similar arguments were developed indicating that the op-amp in the A2 position should determine the speed and bandwidth of the composite. The fact that the composite tolerates mismatching of the GBWP of the individual op-amps allows a slow, bandwidth limited op-amp in the A1 position with a fast, generally less accurate, but large bandwidth op-amp in the A2 position. The result is a fast and accurate composite operational amplifier.

IV. PROGRAMMABLE C2OAS

A. DESIGN PARAMETERS/SPECIFICATIONS

The design for this thesis had the following predetermined specifications. All four of the C2OA forms were to be laid out on the integrated circuit. A range of internal resistor ratios, α, between 1 and 10 would be available and selectable by the user. The number of pins on the chip would ideally be kept to a minimum. Finally, the chip would be CMOS because of the low power consumption and the ability to combine both digital and analog design on the same chip.

All of the requirements listed above were not achieved due primarily to routing limitations. The problems and the trade offs are discussed below. The design parameters were flexible enough to allow for the final design realization to incorporate nearly all of them. The final integrated circuit layout is discussed in Section C.

B. DESIGN PROCEDURES

1. Monochip Concept

The final design of the programmable C2OAs was laid out on Ferranti Interdesign's CMOS Monochip. The Monochip is a unique process that allows rapid design and manufacture of custom integrated circuits [Ref. 2]. For

CMOS analog circuits, there are two sizes of Monochips available, the MLA and the MLB (Figures 4.1, 4.2). Each Monochip is predesigned with a set number of given components. Components include several sizes of NMOS and PMOS transistors, capacitors, and resistors. The transistor components used in development of the programmable C2OAs are shown in Figure 4.3.

The individual designer must know the number and kind of elements required for his design to choose the appropriate Monochip. For this study the MLA Monochip was chosen to meet the component requirements. Once chosen the designer need only draw the interconnections for the components to be used. This information is used to customize the metalization layer to achieve circuit design. The development costs are a fraction of those found in fully customized design. Additionally, the development schedule can be much shorter. The Interdesign company provides a step-by-step manual, Ref. 2, to develop the custom chip. Some of the more relevant steps include circuit design, simulation breadboarding, and chip layout. The design of the Monochip is low risk and straight forward.

Some of the advantages associated with choosing the CMOS Monochip design include virtually zero standby power consumption, established high reliability, and the inclusion of both linear (analog) and digital functions.

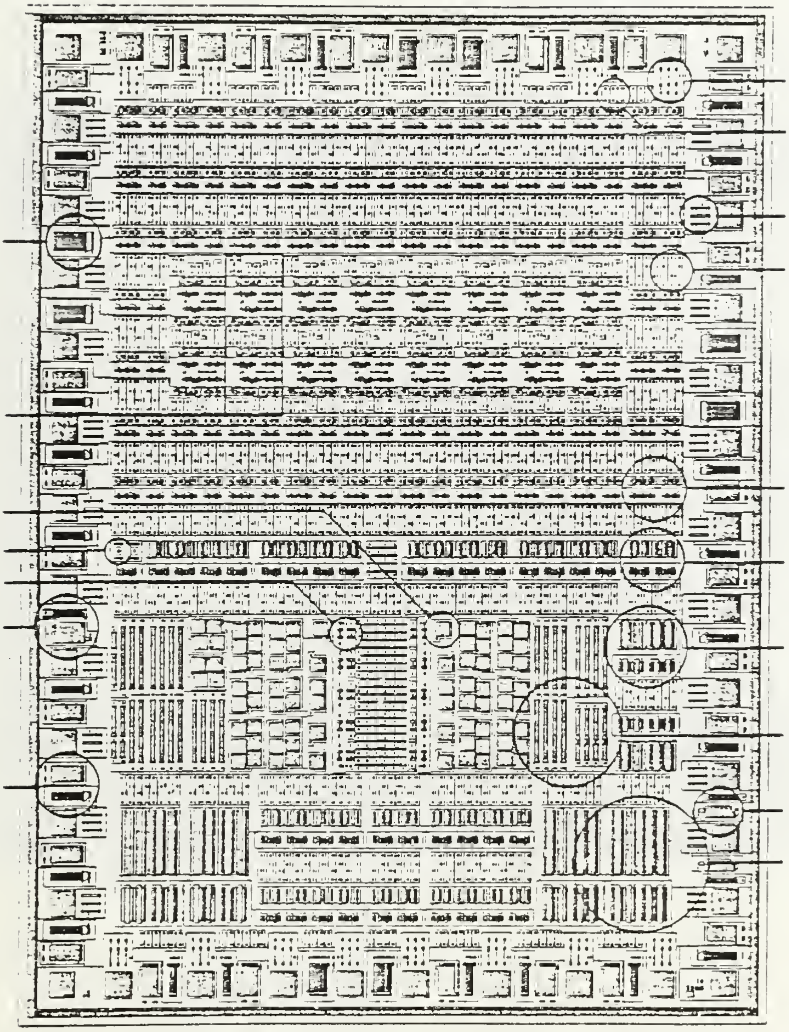


Figure 4.1 Ferranti Interdesign Monochip - MLA

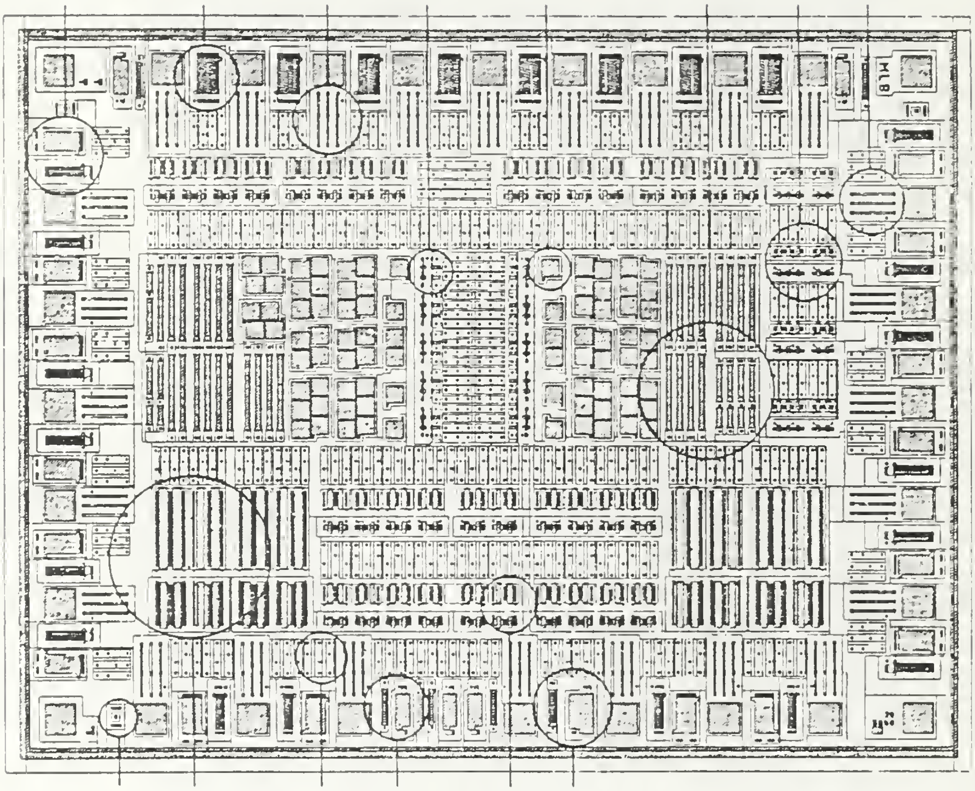
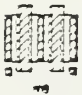
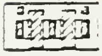
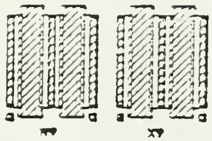
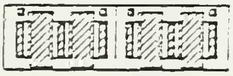


Figure 4.2 Ferranti Interdesign Monochip - MLB

Medium Analog

			MLA	MLB	
Label	Geometry	Gate	Qty	Qty	Applications
B.		P-ch W/L = 60/12	78	78	Medium performance analog circuits such as matched current sources.
		N-ch W/L = 24/12	78	76	

Large Analog

			MLA	
Label	Geometry	Gate Size	Qty	Applications
C.		P-ch W/L = 120/24	8	High performance analog circuits such as active loads for large differential input transistor pairs.
		N-ch W/L = 48/24	8	

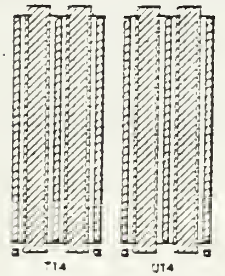
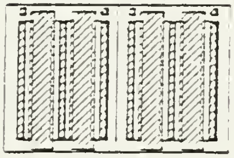
			MLA	MLB	
Label	Geometry	Gate Size	Qty	Qty	Applications
D.		P-ch W/L = 290/24	16	16	High performance analog circuits such as differential input transistor pairs with minimum noise and offset voltage. (P-ch spot noise for two transistors in parallel at $I_{DS} = -10$ microamps is $75nV/\sqrt{Hz}$ at 10Hz).
		N-ch W/L = 155/24	16	16	

Figure 4.3 CMOS Transistor Sizes Used in C20A Construction

2. Circuit Design

Ferranti Interdesign has several CMOS dual inline package [DIP] integrated circuit op-amps available for breadboarding different design ideas. Each op-amp was tested to derive basic properties such as slew rate and offset voltage. In order to have a basis of comparison, one of the available designs was chosen to use as the basic op-amp in the C2OAs. The design selected, CMOS type P1, is shown in Figure 4.4, while the experimental and simulated parameters of this op-amp are discussed in more detail below.

Once an op-amp design was chosen a basic circuit schematic was developed. The initial design had all four C2OAs and a selectable (variable α) group of resistors. This design was partially breadboarded and simulated but then found to be improbable when brought to the layout stage due to routing limitations. The circuit was then redesigned based on the knowledge of component location on the MLA Monochip and routing requirements. As a result, the schematics shown in Figures 4.5 and 4.6 were then chosen to be implemented and their performance was experimentally tested and simulated. These schematics show only three of the four C2OA composite forms. The fourth composite, C2OA-2, was not realized because of routing and component location limitations as discussed below. It should be noted that the 1x 2x 3x numbers in the schematics

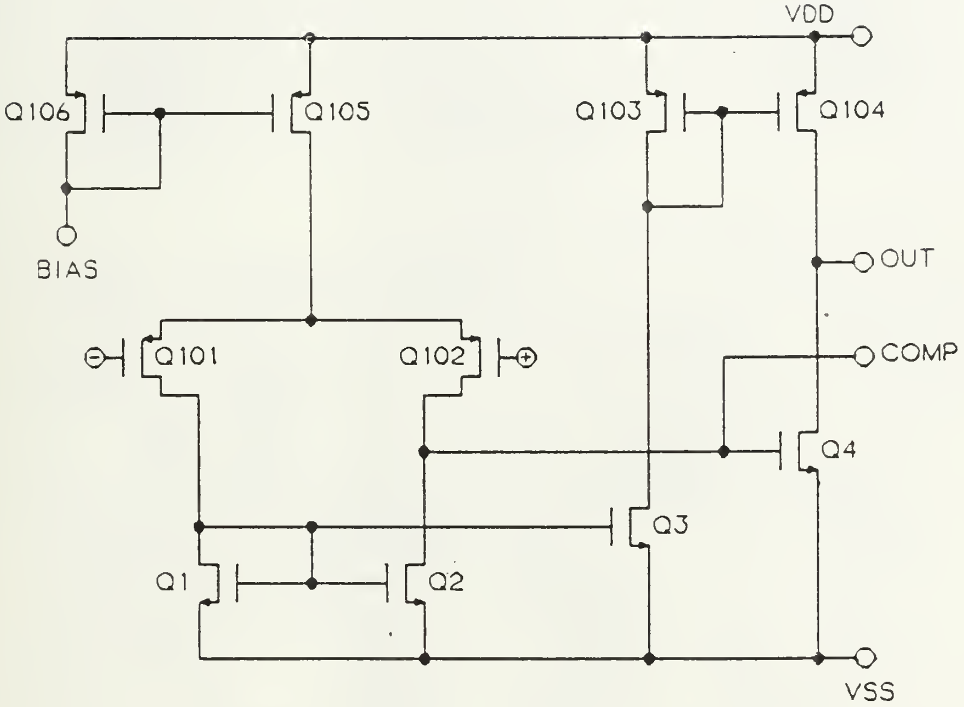


Figure 4.4 Ferranti Interdesign CMOS Op-Amp Type P1

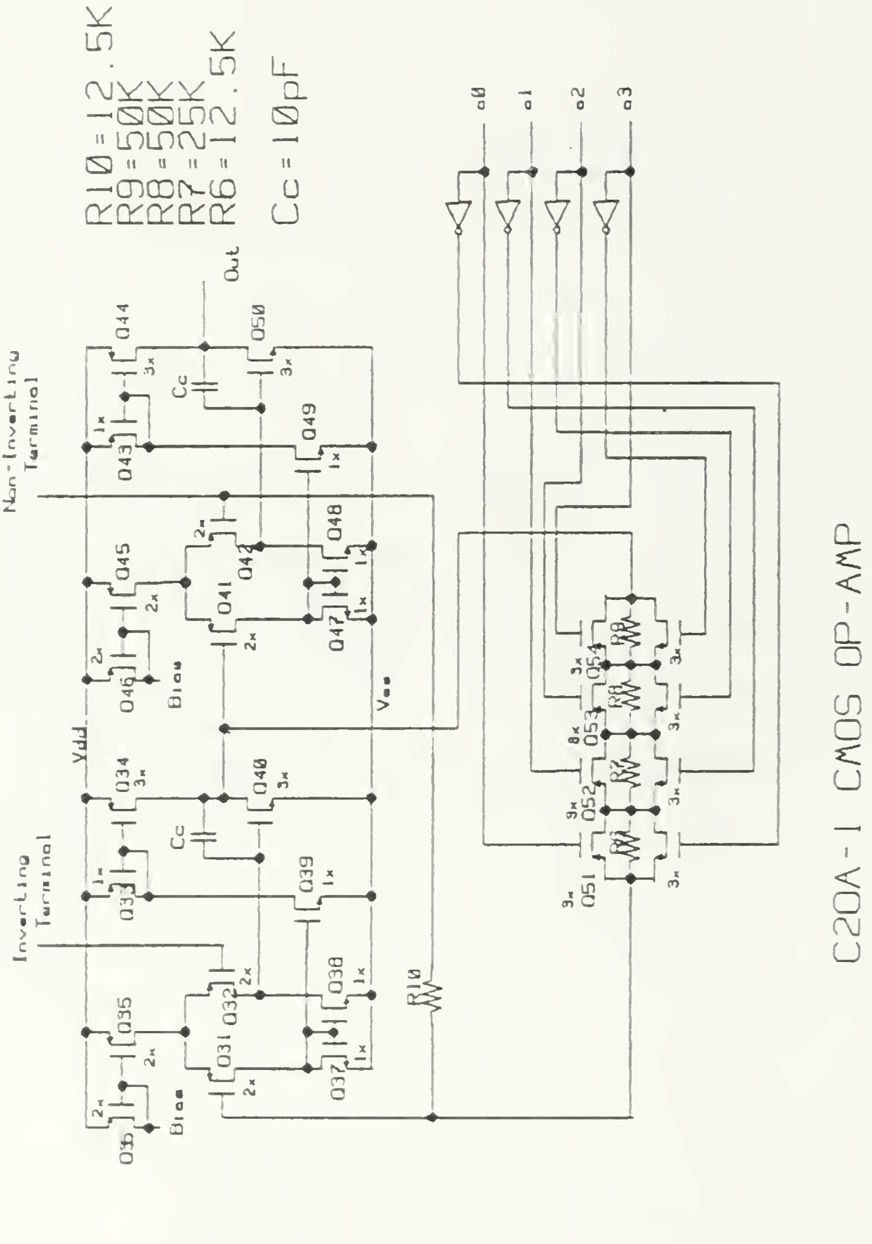


Figure 4.5 C20A-1 Schematic Used for Integrated Circuit Layout

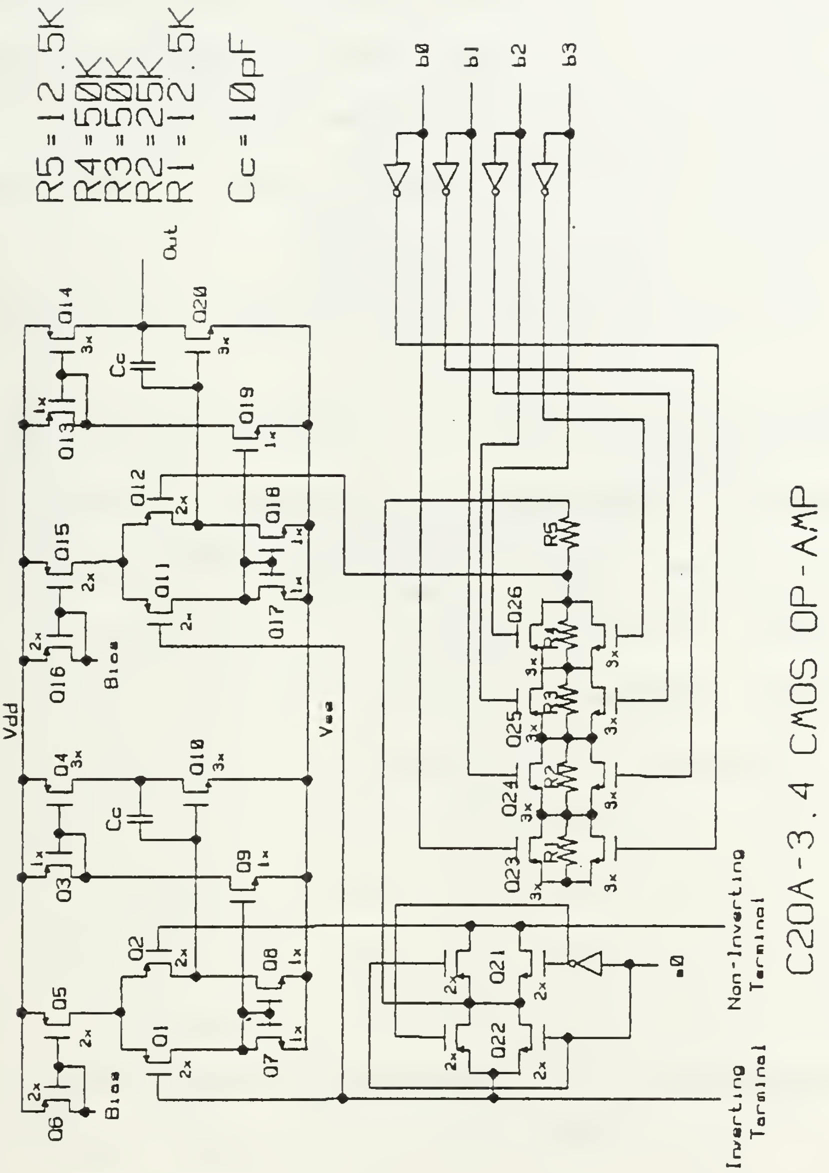


Figure 4.6 C20A-3,4 Schematic Used for Integrated Circuit Layout

indicate the number of paralleled transistors in each of the indicated transistor positions.

The circuit was made programmable by the switchable network of resistors shown in the schematic. The user can select any or all of the resistors to vary the resistance ratio α. Varying α, as was shown in chapter III, has the direct effect of varying Q. Thus the user can vary Q by either opening or shorting the switches on each resistor. A representative illustration of the effect on the frequency response of C20A-1 by varying α is shown in Figure 4.7.

The switches used in the selectable resistor network required additional consideration. Initially the switches were simple NMOS transistors. Because of signal voltage swings, an NMOS switch is unacceptable. As the signal voltage changes, the gate-to-source, V_{GS}, voltage changes. Depending on the magnitude of the signal voltage and the composite configuration, V_{GS} could go below the threshold voltage of the NMOS transistor causing it to turn off. A transmission gate was used to avoid this situation as shown in the schematics of Figures 4.5 and 4.6.

In addition to the type of switch used, the impedance of the switch when used to short circuit its respective resistor must be considered. Simulation showed a variation in the resistance as a function of drain-to-source voltage and current (Figure 4.8). In most practical

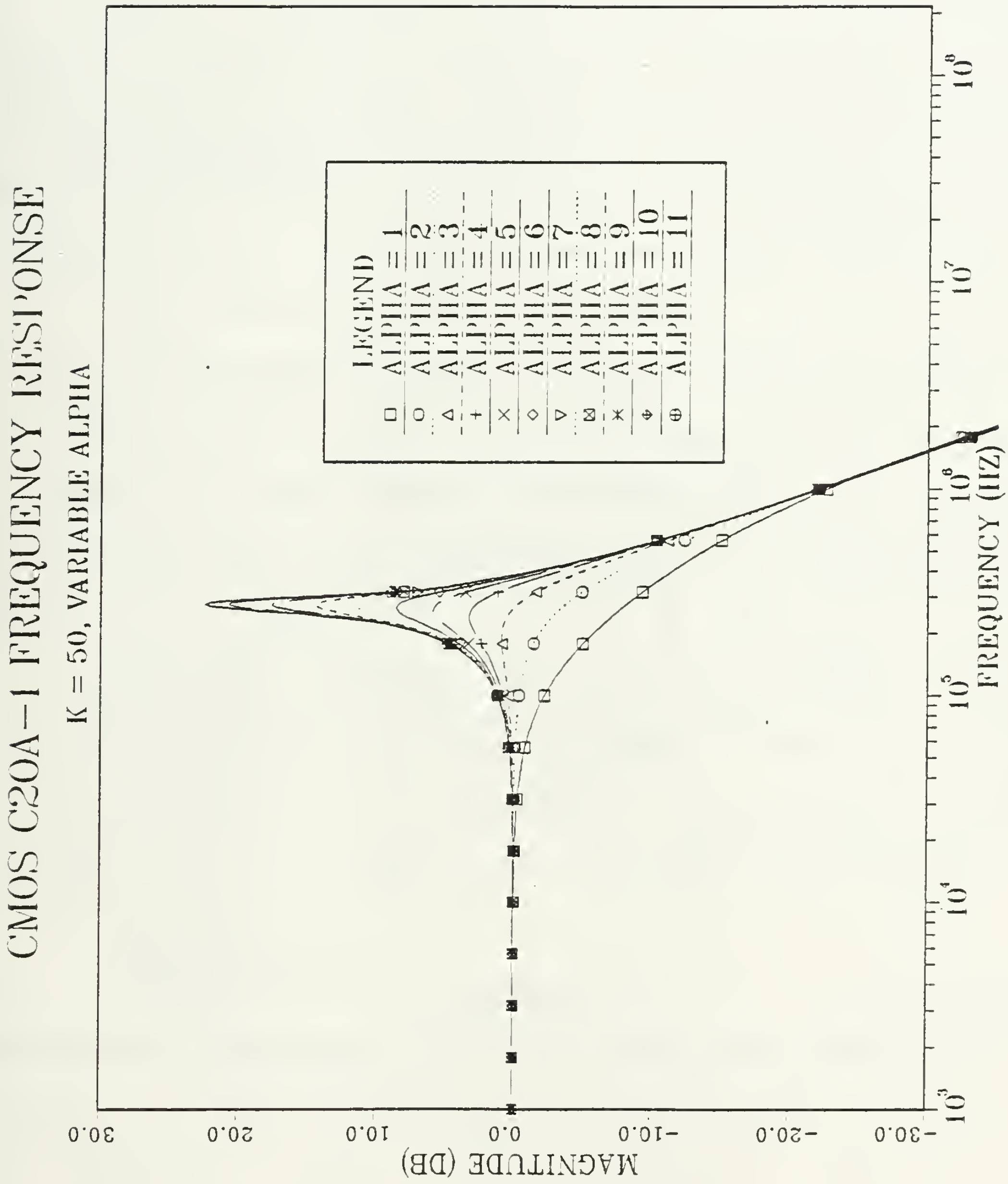


Figure 4.7 C20A-1 Frequency Response With Variable α (Variable Q)

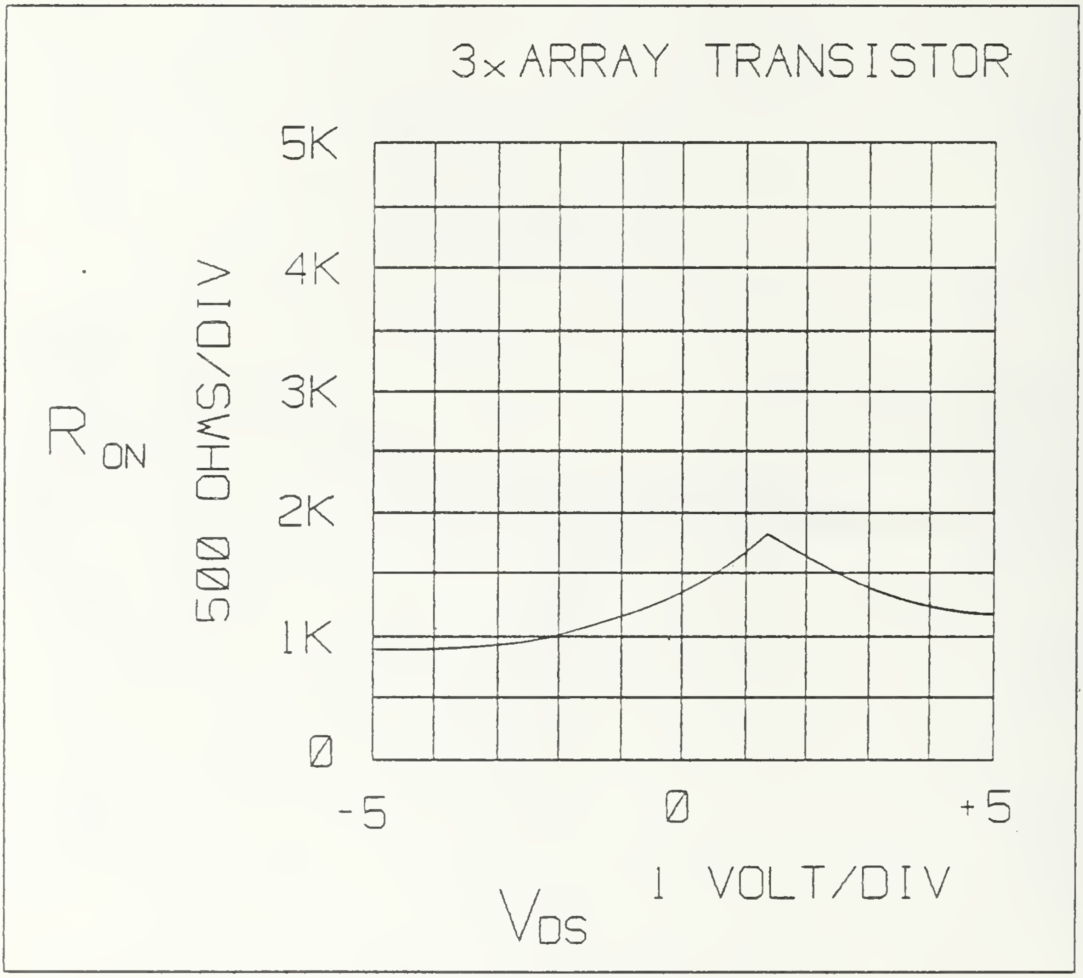


Figure 4.8 Resistance of 3x Switch When "ON" as a Function of V_{DS}

applications the internal node voltages of the composites are small and vary about zero volts. In this situation the impedance of the switch varied little and was approximately 1.2K ohms. However, the impedance across the transistors/switch must be considered if the signal voltage drop across it is large (greater than 1 volt - most commonly seen in the voltage follower configuration). The impedance of the "on" switch can vary by as much as 800 ohms. This will correspond to a changing α and in turn Q. The worst case would be a ten percent variance in Q about the desired value. This study accepted this limitation given that in most op-amp configurations with a gain greater than five, the difference in Q is less than one percent.

The circuit design phase included all of the other phases as trade offs and design changes were made. The final design was a collaboration of routing limitations, component placement limitations, and simulation results.

3. Simulation

The circuit diagrams discussed above and a single CMOS type P1 op-amp were simulated using the Berkeley SPICE version 2G. The listings used for the three C2OAs are in the Appendix. The simulated frequency response and transient response were used to determine the expected slew rate, 3 dB point, and the gain bandwidth product for the final integrated circuit design. Frequency response curves, used in determining the 3 dB point and GBWP, for an inverting finite gain maximally flat configuration are shown in Figures 4.9 through 4.12. The transient response, used to simulate and determine the slew rate, for the composites and a single type P1 op-amp are shown in Figures 4.13 through 4.16. Because of stability requirements, the C20A-1 composite could not be used in the standard voltage follower form for slew rate simulation. It was simulated using a low gain, K=5, inverting configuration.

The equations shown in Figures 3.6 and 3.7 were used to calculate the theoretical offset voltage, 3 dB point, and GBWP. The calculated figures are compared in Figure 4.17 with those found in the SPICE simulation runs. In addition, Figure 4.18 shows a typical increase in bandwidth of the composite over the single operational amplifier.

4. Breadboarding

Prefabricated chips with the standard components available to the designer are used to breadboard the circuit design. Actual performance measurements can then be taken and the circuit adjusted to obtain peak performance. Some common circuit components are also available in prefabricated form. These include several operational amplifiers, digital gates, and switches. These components can also be put into the breadboard circuit. Once optimum performance of the breadboarded components was

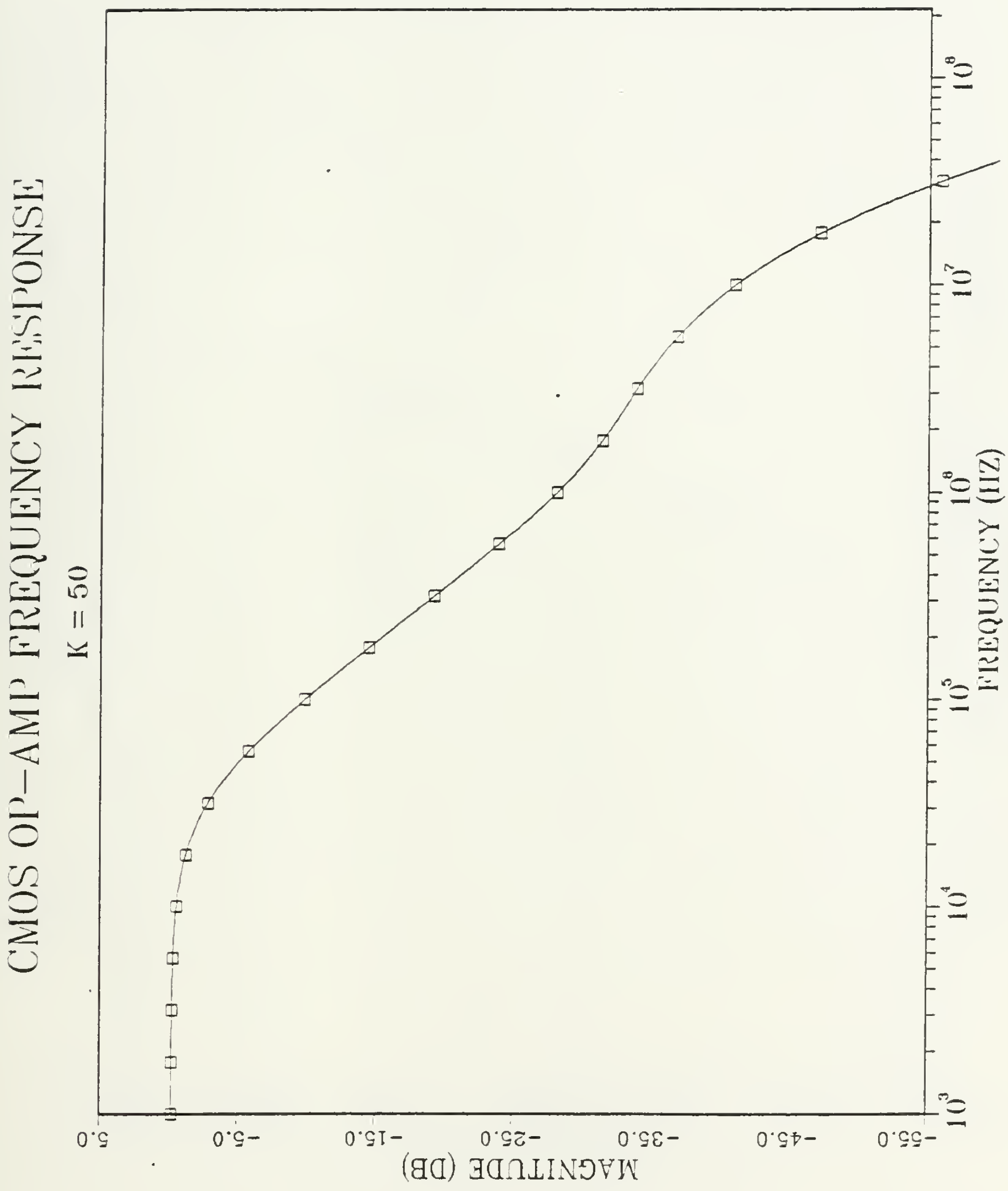


Figure 4.9 SPICE Frequency Response for CMOS Type P1 Op-Amp

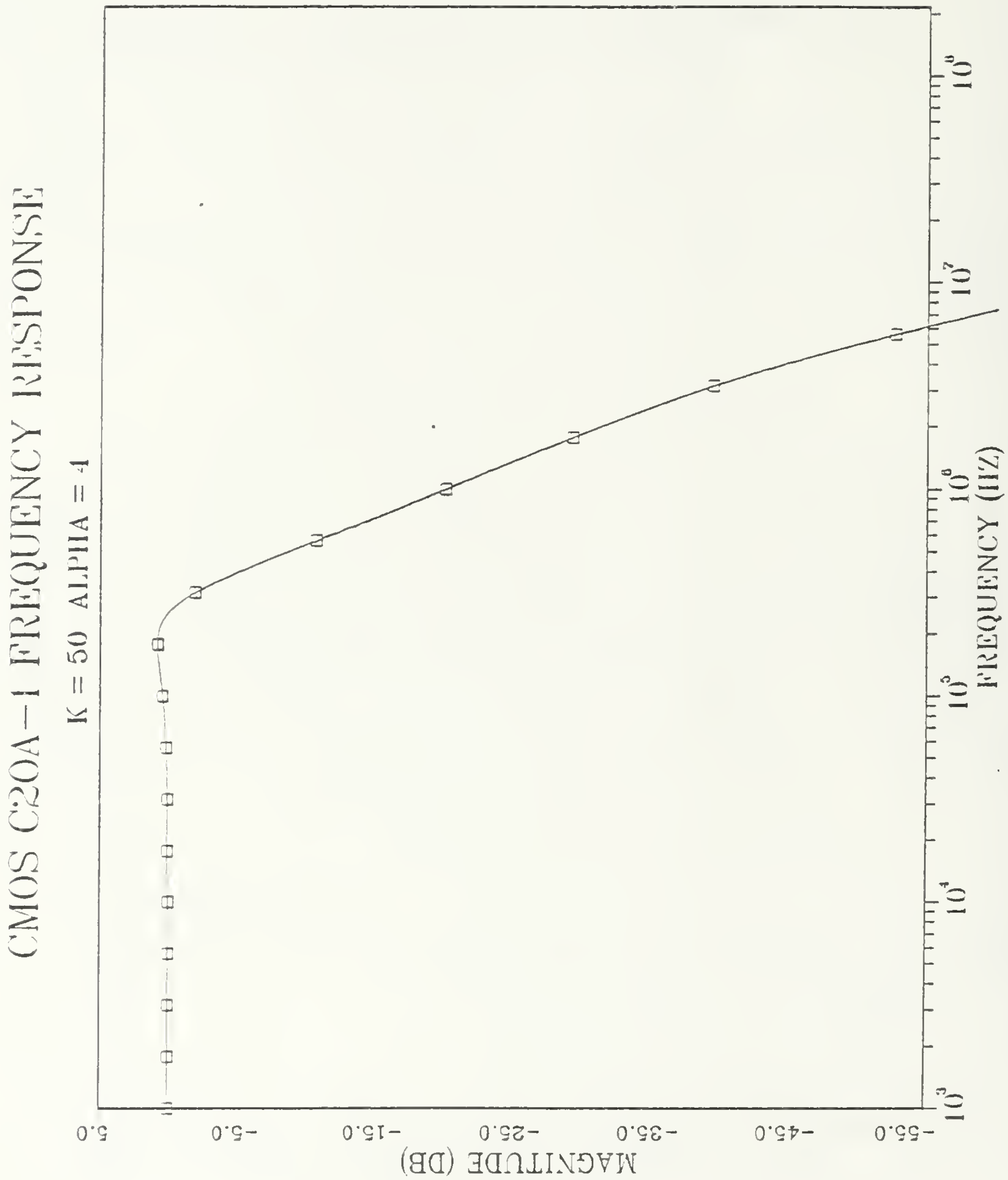


Figure 4.10 SPICE Frequency Response for C20A-1 Op-Amp

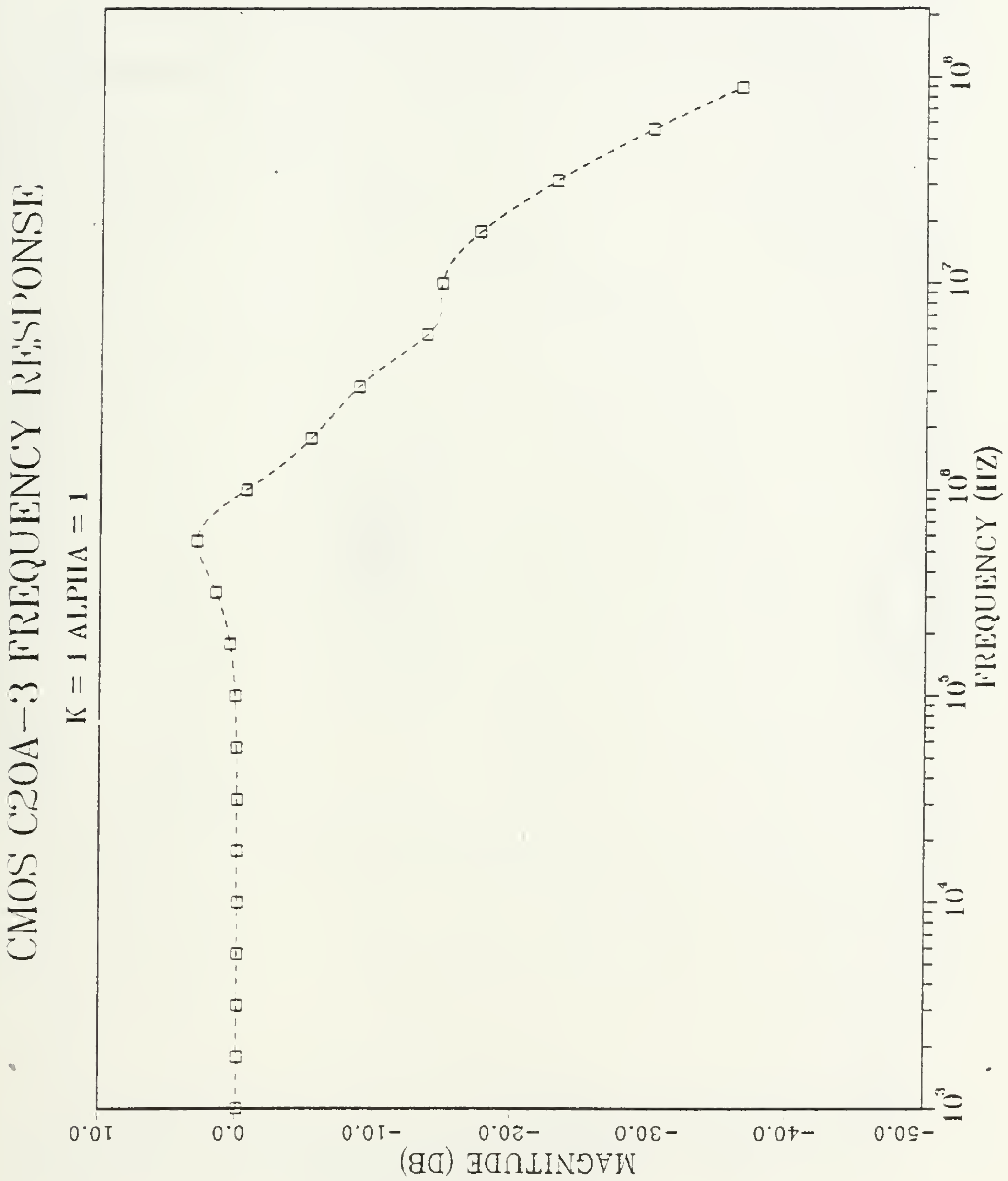


Figure 4.11 SPICE Frequency Response for C20A-3 Op-Amp

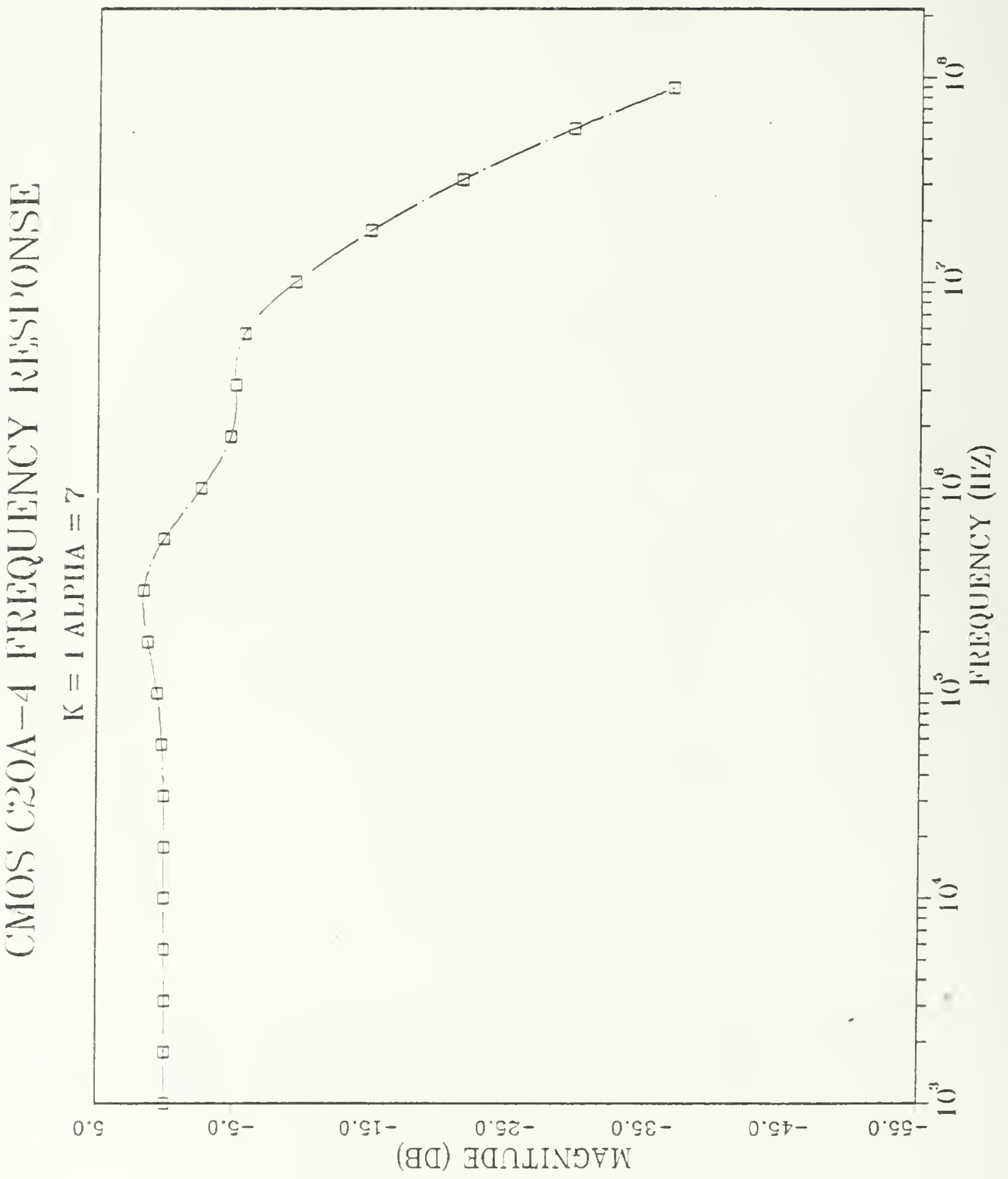


Figure 4.12 SPICE Frequency Response for C2OA-4 Op-Amp

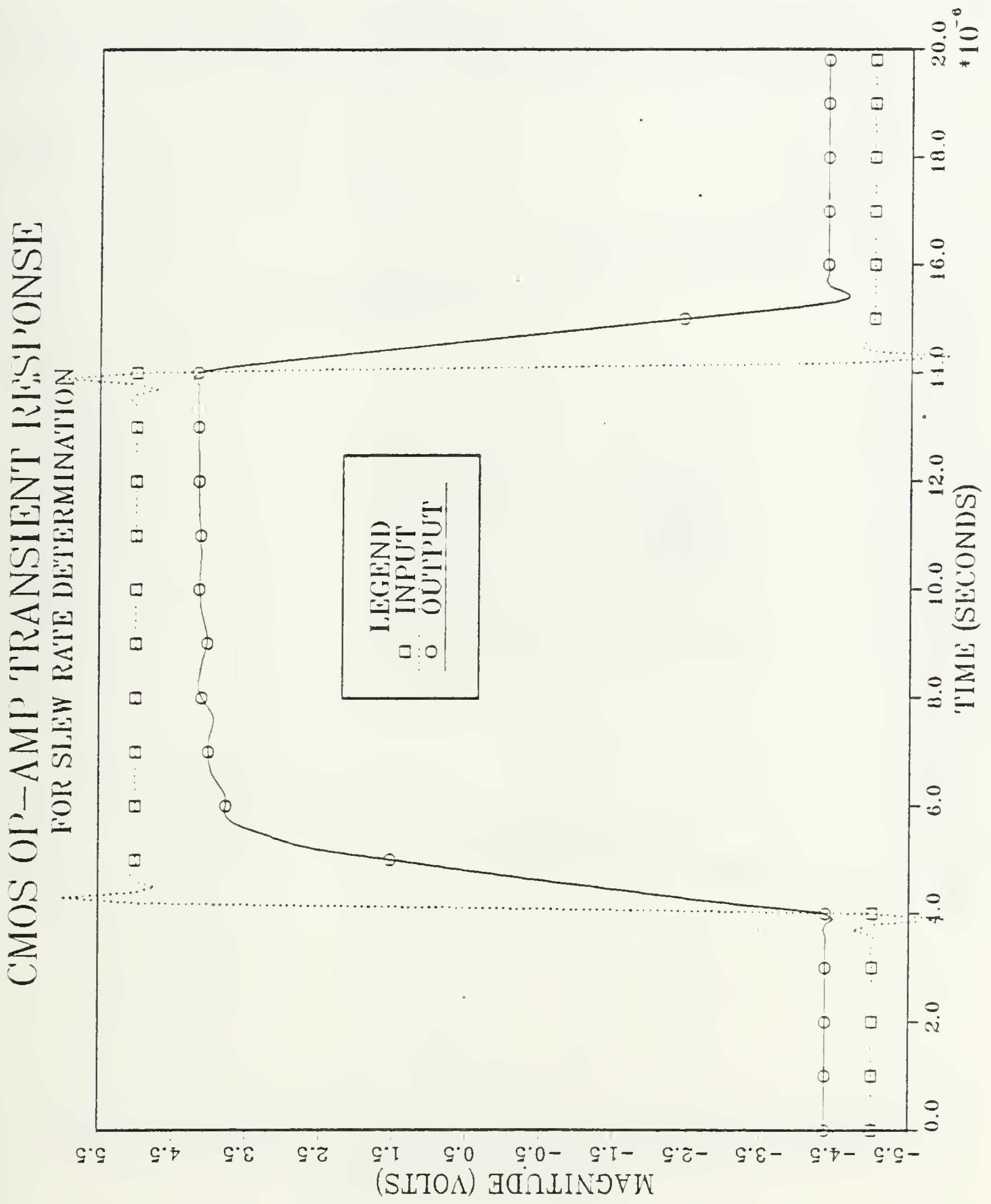


Figure 4.13 SPICE Transient Response for CMOS Type P1 Op-Amp [Voltage Follower]

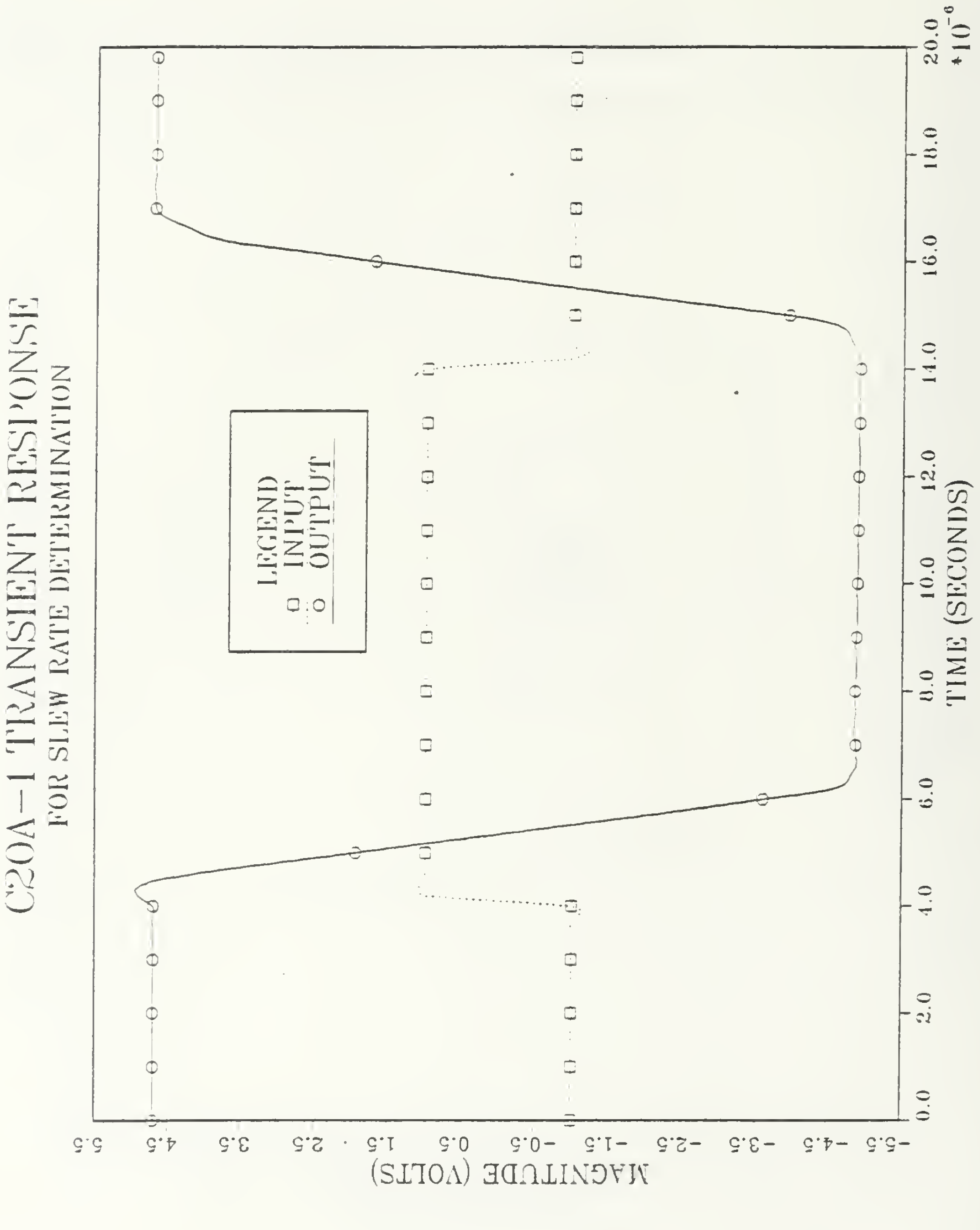


Figure 4.14 SPICE Transient Response for C2OA-1 Op-Amp [Inverting Finite Gain]

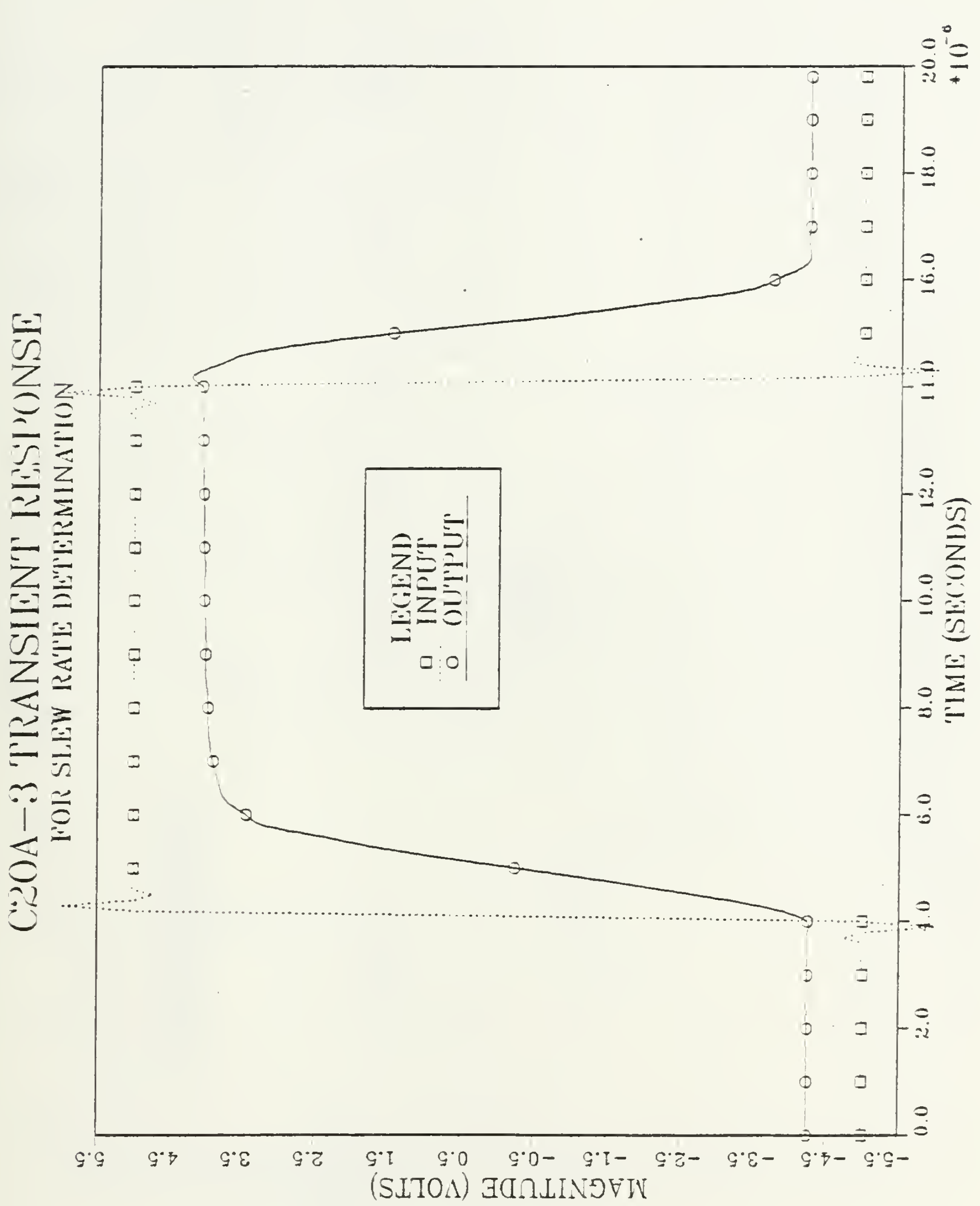


Figure 4.15 SPICE Transient Response for C20A-3 Op-Amp [Voltage Follower]

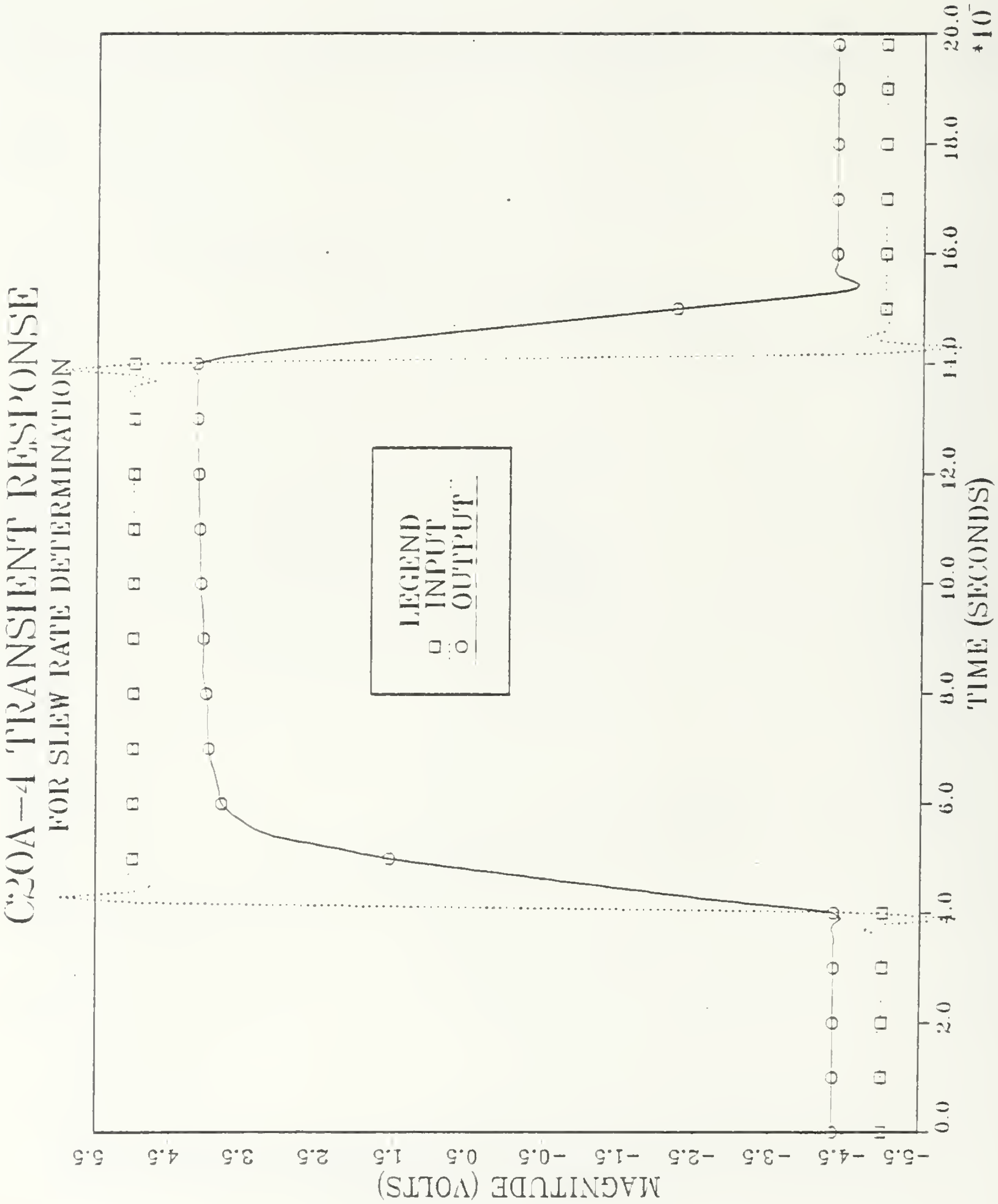


Figure 4.16 SPICE Transient Response for C2OA-4 Op-Amp [Voltage Follower]

	SIMULATION PARAMETERS CMOS TYPE P1 OP-AMP	CLACULATED C20A PARAMETERS *			SIMULATION C20A PARAMETERS		
		C20A-1	C20A-3	C20A-4	C20A-1	C20A-3	C20A-4
OFFSET [mV]	4.12	NA	NA	NA	1.37	1.54	2.45
SLEW RATE [V/microsec]	3.2	NA	NA	NA	5.12	5.68	7.00
3 dB FREQUENCY	3.35×10^4	2.35×10^5	8.4×10^5	8.4×10^5	3.45×10^5	1.3×10^6	6.2×10^5
GBWP	1.68×10^6	1.18×10^7	8.4×10^5	8.4×10^5	1.72×10^7	1.3×10^6	6.2×10^5
K	50	50	1	1	50	1	1
ALPHA	4	4	1	1	4	1	1
Q	0.7	0.7	2	2	0.7	2	2

* Based on results from type P1 op-amp simulation data.

Notes:

Slew rate adjustable with Ibias.

All op-amps have 1x 2x 3x paralleled transistors.
See schematics [Fig. 4.5.4.6]

Figure 4.17 Simulation Results for C20A-1, C20A-3, and C20A-4

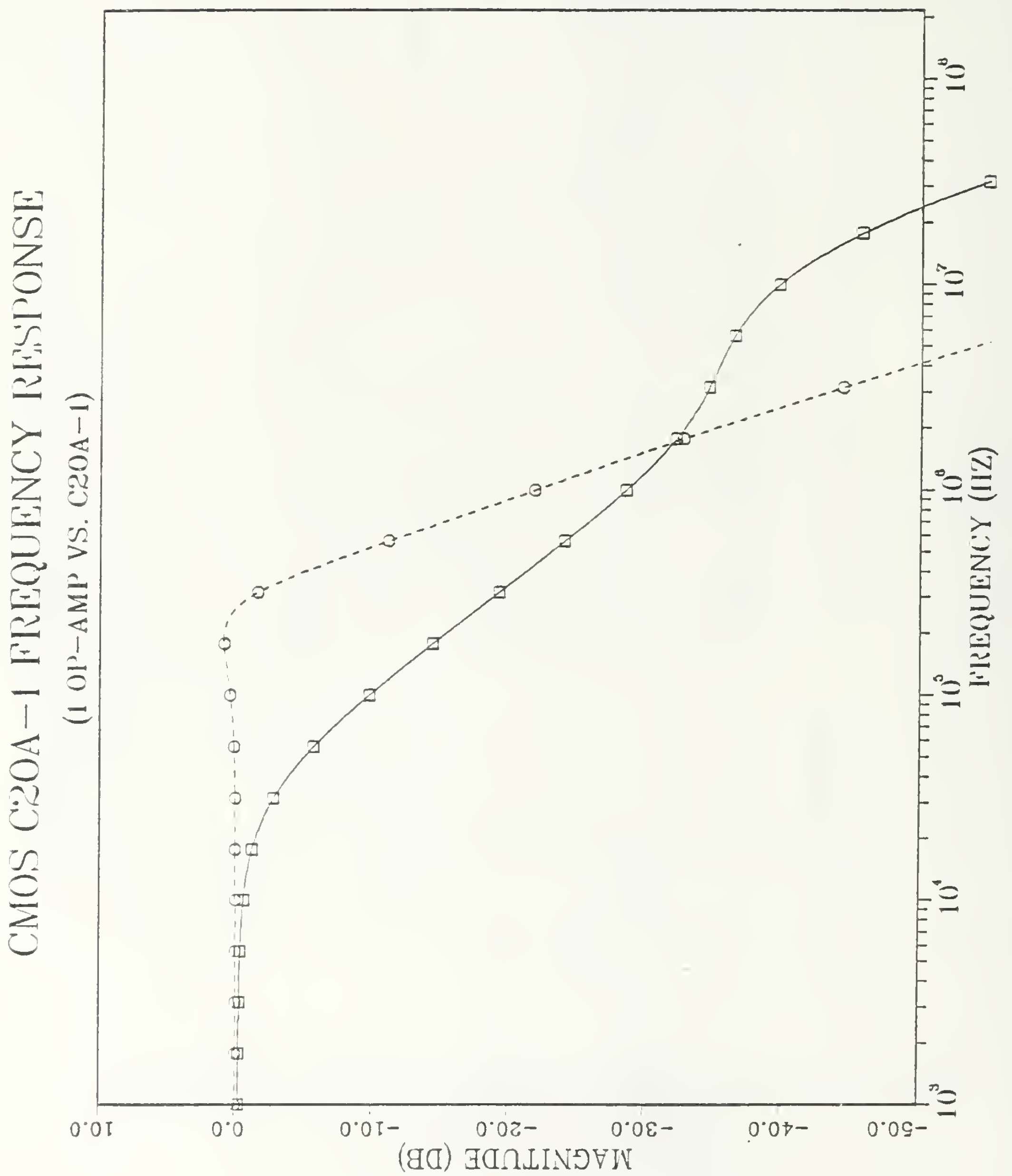


Figure 4.18 One CMOS Op-Amp versus C20A-1 Op-Amp Finite Gain (K=50), Maximally Flat (Q=.7071) Frequency Response

achieved, the circuit diagram used for layout was developed.

As previously mentioned, CMOS op-amps were obtained from Ferranti Interdesign, Inc. The op-amps (Figure 4.4) were wired into the four different C20A forms and then tested using the circuit shown in Figure 4.19. Slew rates and GBWP were measured using the same equipment for each composite form. The equipment used included an oscilloscope (HP 1220A), a dual power supply (HP 6234A), a signal generator (WAVETEK Model 142), and a digital multimeter (TEKTRONIX DM501).

The results from experimentation which include slew rate, GBWP, and offset are listed in Figure 4.20. It must be noted that the transistors in the type P1 op-amp available for breadboarding are the small array transistors on the MLA chip (Figure 4.3). The transistors used in the actual construction of the final product will be of the medium and large analog types (Figure 4.3). This should allow for better performance in the manufactured chip than that achieved in the experimentation shown above. Indeed, simulation shows that performance is noticeably improved using the larger transistors.

5. Layout of Chip

Chip layout is accomplished by using an enlarged photocopy (on mylar) of the actual chip. The designer then uses non-graphite marking pencils to draw the

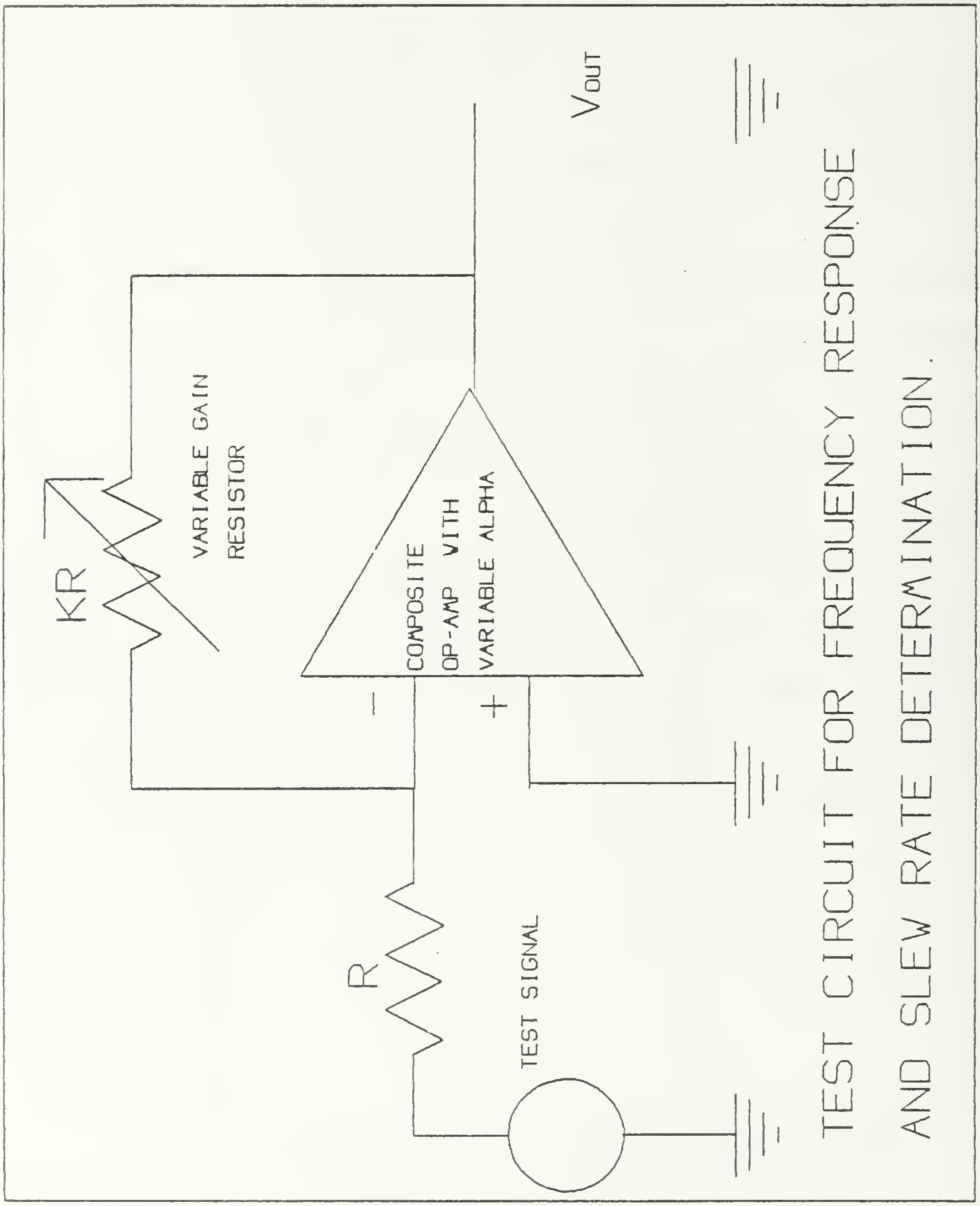

V_OUT
VARIABLE GAIN RESISTOR
KR
COMPOSITE OP-AMP WITH VARIABLE ALPHA
−
+
R
TEST SIGNAL
TEST CIRCUIT FOR FREQUENCY RESPONSE AND SLEW RATE DETERMINATION.

Figure 4.19 Wiring Diagram for Breadboard Testing

	EXPERIMENTAL PARAMETERS CMOS TYPE P1 OP-AMP	CLACULATED C20A PARAMETERS *			EXPERIMENTAL C20A PARAMETERS		
		C20A-1	C20A-3	C20A-4	C20A-1	C20A-3	C20A-4
OFFSET [mV]	10.7	NA	NA	NA	7.3	4	4
SLEW RATE [V/microsec]	3.2	NA	NA	NA	6.5	3	3
3 dB FREQUENCY	2.53×10^{4}	1.76×10^{5}	6.3×10^{5}	6.3×10^{5}	1.5×10^{5}	5.88×10^{5}	5.3×10^{5}
GBWP	1.26×10^{6}	8.82×10^{6}	6.3×10^{5}	6.3×10^{5}	7.8×10^{6}	5.88×10^{5}	5.3×10^{5}
K	50	50	1	1	50	1	1
ALPHA	4	4	1	1	4	1	1
O	0.7	0.7	2	2	0.7	2	2

* Based on results from experimental type P1 op-amp data.

Notes:
Slew rate adjustable with Ibias.
All op-amp transistors are 2x paralleled.

Figure 4.20 Experimentally Determined and Calculated Results for Type P1, C20A-1, C20A-3, and C20A-4

interconnections between circuit components. To ease this potentially tedious job, predrawn overlays are available for the common circuit components found in the breadboarding stage of design. Once all circuit components are interconnected, the layout is sent to Interdesign for digitization, simulation, and, finally, fabrication.

The mylar layout sheet has predrawn grid markings that allow for appropriate spacing of metal lines (12 microns). As is typical of integrated circuit design, interconnect lines must avoid running over other components on the chip. In custom VLSI design, this can be accomplished relatively easily because all components are movable and not already laid in silicon. The Monochip allows for changes in the metal routing only. This restriction caused several changes in the ultimate design. Only two, C20A-1 and C20A-3, composite forms were generated for layout. Of the two, one, C20A-3, was made user-switchable to obtain a third form namely C20A-4. The similarities between C20A-3 and C20A-4 can be readily seen in Figures 3.3 and 3.4. The above constraints were taken back through the breadboard and simulation stages to achieve the results listed in this chapter. The final design and layout sent to be manufactured will be discussed in section 6.

6. Final Layout

The final layout (Figure 4.21) included 200 transistors, 4 capacitors, and 10 resistors. It included connections between four type P1 op-amps in the three available composite forms C2OA-1, C2OA-3, and C2OA-4. Each internal op-amp was allowed a separate bias pin to allow the user to "tweak" the DC bias current on the individual op-amps thereby effecting the open loop gain and slew rate of the op-amp. Each composite op-amp has a user selectable α range between 1 and 12. The α, or internal resistor ratio, is selectable by four control lines to each composites resistor network (Figures 4.6, 4.7).

The composites appear to the user as a normal operational amplifier in that they exhibit the three normal op-amp terminals: an inverting terminal, a non-inverting terminal, and an output terminal. The resultant chip will be packaged in a 24 pin dual inline package.

C. CONCLUSIONS

The implementation of a semi-custom integrated circuit requires several steps all of which are heavily interrelated. The payoffs to using semi-custom are fast manufacture and delivery time. The most significant trade-off is the inability of the chip to support complex circuit routing. The routing capabilities are extremely limiting unless the design is very repetitive using components in

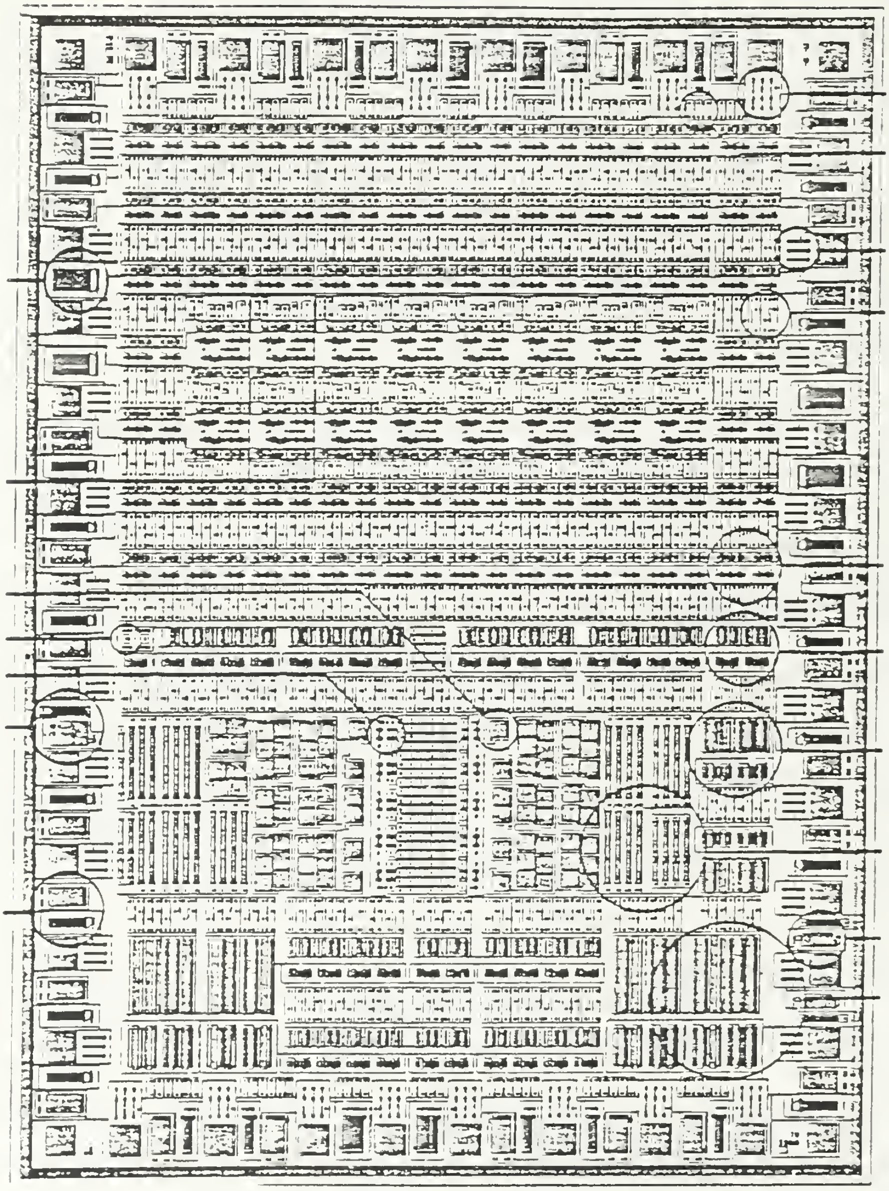


Figure 4.21 Final layout of Programmable CMOS Composite Operational Amplifier

close proximity. The final layout is a conglomeration of all the design steps with many reiterations due to the associated trade-offs and limitations. The semi-custome chip meets all specifications save one. Due to the routing limitations, the composite form C20A-2 was not integrated onto the chip.

V. CONCLUSIONS

The objective of this thesis was to layout programmable composite operational amplifiers on a single integrated circuit. The concept and use of composites is well documented but heretofore never integrated on to a single chip.

The basic operational amplifier parameters of input offset voltage, slew rate limiting, frequency dependent gain, and GBWP were discussed in Chapter I. It was shown that a single operational amplifier that is both fast and accurate is impossible to obtain. This limitation is overcome and the available bandwidth extended by composite operational amplifiers.

Chapter II elaborated on the basic op-amp parameters as they apply to CMOS operational amplifiers. The low transconductance of MOS transistors effects both the slew rate (improving it) and the offset voltage (degrading it). Through various techniques differences between MOS operational amplifiers and bipolar operational amplifiers are minimized. It was shown that the CMOS op-amp can generally be studied in the same manner as its bipolar counterpart.

The concept of composite operational amplifiers and the general approach to their generation was presented in

Chapter III. Composites showed potential for developing high speed, high accuracy, operational amplifiers that extend the useful operating frequencies of linear active networks. Of the 136 different C2OA combinations, four were shown to satisfy the given criteria and deliver superior performance over single op-amps. The C2OA input offset voltage was shown to be approximately the offset of the op-amp occupying the A1 position. The A2 position determines the speed and bandwidth of the composite. The fact that the composite tolerates mismatching of the GBWP of the individual op-amps allows a slow, bandwidth limited op-amp in the A1 position with a fast, generally less accurate, but large bandwidth op-amp in the A2 position. The result is a fast and accurate composite operational amplifier.

Chapter IV discussed the design procedures involved with the Ferranti Interdesign Monochip. The final layout included 200 transistors, 4 capacitors, and 10 resistors. Four type P1 op-amps were interconnected into the three composite forms C2OA-1, C2OA-3, and C2OA-4. Each internal op-amp had a separate bias pin to allow the user to set the DC bias current on the individual op-amps thereby controlling the open loop gain and the slew rate of the op-amp. Each composite op-amp had a user selectable α range between 1 and 12. The individual composites were shown to appear as normal operational amplifiers in that they exhibit an inverting terminal, a non-inverting terminal, and an output terminal. The final design and layout met all specifications except for the elimination of C20A-2 due to routing constraints.

The fast manufacture and delivery time associated with semi-custom integrated circuit design makes it extremely desirable. The related drawbacks are the inability to support complex circuit routing. The design procedure requires several heavily interrelated steps. The final layout incorporated all of the predefined parameters and specifications except one. The routing limitations found during circuit layout limited the final design to only three of the four C20A composite operational amplifiers. The final circuit has all of the desirable characteristics found in composite operational amplifiers.

APPENDIX

SPICE SIMULATION LISTINGS

```
TEST CIRCUIT FOR CMOS OP-AMP P1
.WIDTH IN=80 OUT=80
* .OPT ACCT LIST NODE LIMPTS=1200
* OPTION ABOVE FOR ALL OUTPUT - BELOW FOR FREQ RESPONSE ONLY
.OPT NOMOD LIMPTS=1200
* SUBCIRCUIT ONE STUFF HERE
.SUBCKT OPAMP-P1 8 9 7
.SUBCKT MEDNMOS 1 2 3 4
M1 1 2 3 4 N L=12.0U W=24.0U AD=720P AS=515P PD=108U
+PS=91U NRD=0.25 NRS=0.25
.MODEL N NMOS LEVEL=2 VTO=1.051 TOX=1.0E-7 UO=780 TPG=0
+NSUB=8.25E15 LD=1.9U UCRIT=28400 UEXP=0.10415 UTRA=0.25
+RSH=10 NFS=5.0E11 CJ=2.25E-4 CJSW=6.0E-10 VMAX=4.8E4 NEFF=4.0
+XJ=1.6E-6 CGDO=1.55N CGSO=1.55N CGBO=8.7N
.ENDS MEDNMOS
.SUBCKT MEDPMOS 1 2 3 4
M1 1 2 3 4 P L=12.0U W=60.0U AD=1800P AS=1290P PD=180U
+PS=163U NRD=0.12 NRS=0.12
.MODEL P PMOS LEVEL=2 VTO=-0.915 TOX=1.0E-7 UO=400 TPG=0
+NSUB=5.7E14 LD=1.8U UCRIT=21806.4 UEXP=0.305 UTRA=0.25
+RSH=30 NFS=5.0E11 CJ=1.05E-4 CJSW=3.0E-10 VMAX=5.0E4 NEFF=10.0
+XJ=1.0E-6 CGDO=1.6N CGSO=1.6N CGBO=8.7N
.ENDS MEDPMOS
VDD 1 0  5
VSS 6 0 -5
RB 15 16 50K
VB 16 0 0
* VOFF- 8 0 .0041337
* VOFF+ 9 0 0.0
X6 15 15 1 11 MEDPMOS
X62 15 15 1 11 MEDPMOS
X5 2 15 1 11 MEDPMOS
X52 2 15 1 11 MEDPMOS
X3 5 5 1 11 MEDPMOS
X4 7 5 1 11 MEDPMOS
X42 7 5 1 11 MEDPMOS
X43 7 5 1 11 MEDPMOS
X1 3 8 2 11 MEDPMOS
X12 3 8 2 11 MEDPMOS
X2 4 9 2 11 MEDPMOS
X22 4 9 2 11 MEDPMOS
X7 3 3 6 10 MEDNMOS
X8 4 3 6 10 MEDNMOS
X9 5 3 6 10 MEDNMOS
X10 7 4 6 10 MEDNMOS
X102 7 4 6 10 MEDNMOS
X103 7 4 6 10 MEDNMOS
CINT 7 4 10P
V+GATE 11 1 AC 0.0
V-GATE 10 6 AC 0.0
.ENDS OPAMP-P1
```

Figure A.1 Spice Simulation Listing - 1 for CMOS Type P1 Operational Amplifier

```
XI 3 2 3 OPAMP-R1
* RF 1 3 500K
* RI 4 1 10K
* VIN 4 0 AC .02
* VGND 2 0 0
*
* THIS IS THE PULSE VOLTAGE FOR SLEW RATE DETERMINATION
*
VIN+ 2 0 PULSE (-5 5 4US 2NS 2NS 10US 20US)
*
* THESE ARE THE OUTPUT CARDS
*
.TRAN .2US 24US
.PLOT TRAN V(2) V(3)
.PRINT TRAN V(2) V(3)
* .AC DEC 200 10K 10MEG
* .PRINT AC V(3) VDB(3) V(2) V(1) V(4)
* .PLOT AC VDB(3)
.END
```

Figure A.2 Continuation of Listing - 1

```
TEST CIRCUIT FOR CMOS OP-AMP C20A-1 P1
.WIOTH IN=80 OUT=80
* .OPT ACCT LIST NODE LIMPTS=1200
*
* THE OPTIONS ABOVE FOR ALL OUTPUT - BELOW FOR
* FREQ/TRAN RESPONSE OATA ONLY
*
.OPT NOMOO LIMPTS=1200
* THIS IS THE SIMULATEO OFFSET VOLTAGE
*
* VOFF+ 6 0 0.001878
*
* THIS IS THE SUBCIRCUIT FOR OP-AMP IN A1 POSITION
*
.SUBCKT OPAMP-P1 8 9 7
.SUBCKT MEONMOS 1 2 3 4
M1 1 2 3 4 N L=12.0U W=24.0U AD=720P AS=515P PD=108U
+PS=91U NRD=0.25 NRS=0.25
.MODEL N NMOS LEVEL=2 VTO=1.051 TOX=1.0E-7 UO=780 TPG=0
+NSUB=8.25E15 LD=1.9U UCRIT=28400 UEXP=0.10415 UTRA=0.25
+RSH=10 NFS=5.0E11 CJ=2.25E-4 CJSW=6.0E-10 VMAX=4.8E4 NEFF=4.0
+XJ=1.6E-6 CGDO=1.55N CGSO=1.55N CGBO=8.7N
.ENOS MEDNMOS
.SUBCKT MEDPMOS 1 2 3 4
M1 1 2 3 4 P L=12.0U W=60.0U AO=1800P AS=1290P PO=180U
+PS=163U NRO=0.12 NRS=0.12
.MODEL P PMOS LEVEL=2 VTO=-0.915 TOX=1.0E-7 UO=400 TPG=0
+NSUB=5.7E14 LO=1.8U UCRIT=21806.4 UEXP=0.305 UTRA=0.25
+RSH=30 NFS=5.0E11 CJ=1.05E-4 CJSW=3.0E-10 VMAX=5.0E4 NEFF=10.0
+XJ=1.0E-6 CGOO=1.6N CGSO=1.6N CGBO=8.7N
.ENOS MEOPMOS
VOO 1 0  5
VSS 6 0 -5
RB 15 16 50K
VB 16 0 0
* VOFF- 8 0 .0041337
* VOFF+ 9 0 0.0
X36 15 15 1 11 MEDPMOS
X362 15 15 1 11 MEDPMOS
X35 2 15 1 11 MEOPMOS
X352 2 15 1 11 MEOPMOS
X33 5 5 1 11 MEDPMOS
X34 7 5 1 11 MEOPMOS
X342 7 5 1 11 MEDPMOS
X343 7 5 1 11 MEDPMOS
X31 3 8 2 11 MEDPMOS
X312 3 8 2 11 MEDPMOS
X32 4 9 2 11 MEDPMOS
X322 4 9 2 11 MEOPMOS
X37 3 3 6 10 MEONMOS
X38 4 3 6 10 MEDNMOS
X39 5 3 6 10 MEONMOS
X40 7 4 6 10 MEONMOS
X402 7 4 6 10 MEDNMOS
X403 7 4 6 10 MEONMOS
```

Figure A.3 Spice Simulation Listing - 2 for C20A-1 Operational Amplifier

```
CINT 7 4 10P
V+GATE 11 1 AC 0.0
V-GATE 10 6 AC 0.0
.ENDS OPAMP-P1
*
* THIS IS THE SUBCIRCUIT FOR OP-AMP IN A2 POSITION
*
.SUBCKT OPAMP-P2 8 9 7
.SUBCKT MEDPMOS 1 2 3 4
M1 1 2 3 4 P L=12.0U W=60.0U AD=1800P AS=1290P PD=180U
+PS=163U NRD=0.12 NRS=0.12
.MODEL P PMOS LEVEL=2 VTO=-0.915 TOX=1.0E-7 UO=400 TPG=0
+NSUB=5.7E14 LD=1.8U UCRIT=21806.4 UEXP=0.305 UTRA=0.25
+RSH=30 NFS=5.0E11 CJ=1.05E-4 CJSW=3.0E-10 VMAX=5.0E4 NEFF=10.0
+XJ=1.0E-6 CGDO=1.6N CGSO=1.6N CGBO=8.7N
.ENDS MEDPMOS
.SUBCKT LGNMOS 1 2 3 4
M1 1 2 3 4 N L=24.0U W=155.0U AD=4650P AS=3335P PD=370U
+PS=353U NRD=0.08 NRS=0.08
.MODEL N NMOS LEVEL=2 VTO=1.051 TOX=1.0E-7 UO=780 TPG=0
+NSUB=8.25E15 LD=1.9U UCRIT=29400 UEXP=0.10415 UTRA=0.25
+RSH=10 NFS=5.0E11 CJ=2.25E-4 CJSW=6.0E-10 VMAX=4.8E4 NEFF=4.0
+XJ=1.6E-6 CGDO=1.55N CGSO=1.55N CGBO=7.6N
.ENDS LGNMOS
.SUBCKT LGPMOS 1 2 3 4
M1 1 2 3 4 P L=24.0U W=290.0U AD=8700P AS=6235P PD=640U
+PS=623U NRD=0.1 NRS=0.1
.MODEL P PMOS LEVEL=2 VTO=-0.915 TOX=1.0E-7 UO=400 TPG=0
+NSUB=5.7E14 LD=1.8U UCRIT=21806.4 UEXP=0.305 UTRA=0.25
+RSH=30 NFS=5.0E11 CJ=1.05E-4 CJSW=3.0E-10 VMAX=5.0E4 NEFF=10.0
+XJ=1.0E-6 CGDO=1.6N CGSO=1.6N CGBO=7.5N
.ENDS LGPMOS
VDD 1 0  5
VSS 6 0 -5
RB 15 16 50K
VB 16 0 0
* VOFF- 8 0 .0041337
* VOFF+ 9 0 0.0
X46 15 15 1 11 MEDPMOS
X462 15 15 1 11 MEDPMOS
X45 2 15 1 11 MEDPMOS
X452 2 15 1 11 MEDPMOS
X43 5 5 1 11 LGPMOS
X44 7 5 1 11 LGPMOS
X442 7 5 1 11 LGPMOS
X443 7 5 1 11 LGPMOS
X41 3 8 2 11 LGPMOS
X412 3 8 2 11 LGPMOS
X42 4 9 2 11 LGPMOS
X422 4 9 2 11 LGPMOS
X47 3 3 6 10 LGNMOS
X48 4 3 6 10 LGNMOS
X49 5 3 6 10 LGNMOS
X50 7 4 6 10 LGNMOS
X502 7 4 6 10 LGNMOS
X503 7 4 6 10 LGNMOS
```

Figure A.4 Continuation of Listing - 2

```
CINT 7 4 10P
V+GATE 11 1 AC 0.0
V-GATE 10 6 AC 0.0
.ENDS OPAMP-P2
*
* THIS IS THE MAIN CIRCUIT
*
X1 1 4 2 OPAMP-P1
X2 2 6 3 OPAMP-P2
R10 1 6 12.5K
* THESE ARE THE VARIABLE ALPHA RESISTORS
* RA6 1 7 50K
RA7 1 2 50K
* RA8 8 9 25K
* RA9 9 2 12.5K
RF 4 3 500K
RI 5 4 10K
*
* THIS IS THE PULSE VOLTAGE FOR SLEW RATE DETERMINATION
* REMEMBER THAT 1+ALPHA < (1+K)/2 FOR STABILITY
*
* VIN- 5 0 PULSE (-1 1 4US 2NS 2NS 10US 20US)
VIN+ 6 0 0
*
* THIS IS THE INPUT VOLTAGE FOR FINITE GAIN - GAIN
* BANDWIDTH PRODUCT DETERMINATION K=50, ALPHA=4
*
VIN- 5 0 AC .02
* THESE ARE THE OUTPUT CARDS
* .TRAN .2US 24US
* .PLOT TRAN V(5) V(3)
* .PRINT TRAN V(5) V(3)
.AC DEC 200 10K 10MEG
.PRINT AC V(3) VDB(3) V(2) V(1) V(4)
.END
```

Figure A.5 Continuation of Listing - 2

```
TEST CIRCUIT FOR CMOS OP-AMP C2CA-3 P1
.WIDTH IN=80 OUT=80
* .OPT ACCT LIST NODE LIMPTS=1200
*
* THE OPTIONS ABOVE FOR ALL OUTPUT - BELOW FOR
* FREQ/TRAN RESPONSE DATA ONLY
*
.OPT NOMOD LIMPTS=1200
*
* THIS IS THE SUBCIRCUIT FOR OP-AMP IN A1 AND A2 POSITION
*
.SUBCKT OPAMP-P1 8 9 7
.SUBCKT MEDNMOS 1 2 3 4
M1 1 2 3 4 N L=12.0U W=24.0U AD=720P AS=515P PD=108U
+PS=91U NRD=0.25 NRS=0.25
.MODEL N NMOS LEVEL=2 VTO=1.051 TOX=1.0E-7 UO=780 TPG=0
+NSUB=8.25E15 LD=1.9U UCRIT=28400 UEXP=0.10415 UTRA=0.25
+RSH=10 NFS=5.0E11 CJ=2.25E-4 CJSW=6.0E-10 VMAX=4.8E4 NEFF=4.0
+XJ=1.6E-6 CGDO=1.55N CGSO=1.55N CGBO=8.7N
.ENDS MEDNMOS
.SUBCKT MEDPMOS 1 2 3 4
M1 1 2 3 4 P L=12.0U W=60.0U AD=1800P AS=1290P PD=180U
+PS=163U NRD=0.12 NRS=0.12
.MODEL P PMOS LEVEL=2 VTO=-0.915 TOX=1.0E-7 UO=400 TPG=0
+NSUB=5.7E14 LD=1.8U UCRIT=21806.4 UEXP=0.305 UTRA=0.25
+RSH=30 NFS=5.0E11 CJ=1.05E-4 CJSW=3.0E-10 VMAX=5.0E4 NEFF=10.0
+XJ=1.0E-6 CGDO=1.6N CGSO=1.6N CGBO=8.7N
.ENDS MEDPMOS
VDD 1 0  5
VSS 6 0 -5
RB 15 16 50K
VB 16 0 0
*
* VOFF- 8 0 .0041337
* THIS IS THE SIMULATED OFFSET VOLTAGE
*
X6 15 15 1 11 MEDPMOS
X62 15 15 1 11 MEDPMOS
X5 2 15 1 11 MEDPMOS
X52 2 15 1 11 MEDPMOS
X3 5 5 1 11 MEDPMOS
X4 7 5 1 11 MEDPMOS
X42 7 5 1 11 MEDPMOS
X43 7 5 1 11 MEDPMOS
X1 3 8 2 11 MEDPMOS
X12 3 8 2 11 MEDPMOS
X2 4 9 2 11 MEDPMOS
X22 4 9 2 11 MEDPMOS
X7 3 3 6 10 MEDNMOS
X8 4 3 6 10 MEDNMOS
X9 5 3 6 10 MEDNMOS
X10 7 4 6 10 MEDNMOS
X102 7 4 6 10 MEDNMOS
X103 7 4 6 10 MEDNMOS
```

Figure A.6 Spice Simulation Listing - 3 for C20A-3 Operational Amplifier

```
CINT 7 4 10P
V+GATE 11 1 AC 0.0
V-GATE 10 6 AC 0.0
.ENDS OPAMP-P1
*
* THIS IS THE MAIN CIRCUIT
*
X1 4 6 1 OPAMP-P1
X2 4 2 3 OPAMP-P1
RF 4 3 10K
RI 5 4 10K
R10 2 4 12.5K
*
* THESE ARE THE VARIABLE ALPHA RESISTORS
*
* RA6 1 7 50K
* RA7 1 2 50K
* RA8 1 9 25K
RA9 1 2 12.5K
*
* THIS IS THE INPUT VOLTAGE FOR FINITE GAIN - GAIN
* BANDWIDTH PRODUCT DETERMINATION K=1, ALPHA=1
*
VIN+ 6 0 0.0
VIN- 5 0 AC 1
*
* THIS IS THE PULSE VOLTAGE FOR SLEW RATE DETERMINATION
* REMEMBER THAT 1+ALPHA > (1+K) FOR STABILITY - VOLTAGE FOLLOWER
*
* VIN+ 6 0 PULSE (-5 5 4US 2NS 2NS 10US 20US)
*
* THESE ARE THE OUTPUT CARDS
*
* .TRAN .2US 24US
* .PLOT TRAN V(6) V(3)
* .PRINT TRAN V(6) V(3)
.AC DEC 200 10K 10MEG
.PRINT AC V(3) VDB(3) V(2) V(1) V(4)
.END
```

Figure A.7 Continuation of Listing - 3

```
TEST CIRCUIT FOR CMOS OP-AMP C2OA-4 P1
.WIDTH IN=80 OUT=80
* .OPT ACCT LIST NODE LIMPTS=1200
*
* THE OPTIONS ABOVE FOR ALL OUTPUT - BELOW FOR
* FREQ/TRAN RESPONSE DATA ONLY
*
.OPT NOMOD LIMPTS=1200
*
* THIS IS THE SUBCIRCUIT FOR OP-AMP IN A1 AND A2 POSITION
*
.SUBCKT OPAMP-P1 8 9 7
.SUBCKT MEDNMOS 1 2 3 4
M1 1 2 3 4 N L=12.0U W=24.0U AD=720P AS=515P PD=108U
+PS=91U NRD=0.25 NRS=0.25
.MODEL N NMOS LEVEL=2 VTO=1.051 TOX=1.0E-7 UO=780 TPG=0
+NSUB=8.25E15 LD=1.9U UCRIT=28400 UEXP=0.10415 UTRA=0.25
+RSH=10 NFS=5.0E11 CJ=2.25E-4 CJSW=6.0E-10 VMAX=4.8E4 NEFF=4.0
+XJ=1.6E-6 CGDO=1.55N CGSO=1.55N CGBO=8.7N
.ENDS MEDNMOS
.SUBCKT MEDPMOS 1 2 3 4
M1 1 2 3 4 P L=12.0U W=60.0U AD=1800P AS=1290P PD=180U
+PS=163U NRD=0.12 NRS=0.12
.MODEL P PMOS LEVEL=2 VTO=-0.915 TOX=1.0E-7 UO=400 TPG=0
+NSUB=5.7E14 LD=1.8U UCRIT=21806.4 UEXP=0.305 UTRA=0.25
+RSH=30 NFS=5.0E11 CJ=1.05E-4 CJSW=3.0E-10 VMAX=5.0E4 NEFF=10.0
+XJ=1.0E-6 CGDO=1.6N CGSO=1.6N CGBO=8.7N
.ENDS MEDPMOS
VDD 1 0  5
VSS 6 0 -5
RB 15 16 50K
VB 16 0 0
*
* VOFF- 8 0 .0041337
* THIS IS THE SIMULATED OFFSET VOLTAGE
*
X6 15 15 1 11 MEDPMOS
X62 15 15 1 11 MEDPMOS
X5 2 15 1 11 MEDPMOS
X52 2 15 1 11 MEDPMOS
X3 5 5 1 11 MEDPMOS
X4 7 5 1 11 MEDPMOS
X42 7 5 1 11 MEDPMOS
X43 7 5 1 11 MEDPMOS
X1 3 8 2 11 MEDPMOS
X12 3 8 2 11 MEDPMOS
X2 4 9 2 11 MEDPMOS
X22 4 9 2 11 MEDPMOS
X7 3 3 6 10 MEDNMOS
X8 4 3 6 10 MEDNMOS
X9 5 3 6 10 MEDNMOS
X10 7 4 6 10 MEDNMOS
X102 7 4 6 10 MEDNMOS
X103 7 4 6 10 MEDNMOS
```

Figure A.8 Spice Simulation Listing - 4 for C2OA-4 Operational Amplifier

```
CINT 7 4 IOP
V+GATE 11 1 AC 0.0
V-GATE 10 6 AC 0.0
.ENOS CPAMP-P1
*
* THIS IS THE MAIN CIRCUIT
*
X1 4 6 1 OPAMP-PI
X2 4 2 3 OPAMP-PI
RF 4 3 10K
RI 5 4 10K
R10 2 6 12.5K
*
* THESE ARE THE VARIABLE ALPHA RESISTORS
*
* RA6 I 7 50K
RA7 1 9 50K
RA8 9 8 25K
RA9 8 2 12.5K
*
* THIS IS THE INPUT VOLTAGE FOR FINITE GAIN - GAIN
* BANOWIDTH PROOUCT OETERHINATION K=1, ALPHA=7
*
VIN+ 6 0 0.0
VIN- 5 0 AC I
*
* THIS IS THE PULSE VOLTAGE FOR SLEW RATE DETERMINATION
* REHEHBER THAT 1+ALPHA > 4*(1+K) FOR STABILITY - VOLTAGE FOLLOWER
*
* VIN+ 6 0 PULSE (-5 5 4US 2NS 2NS 10US 20US)
*
* THESE ARE THE OUTPUT CARDS
*
* .TRAN .2US 24US
* .PLOT TRAN V(6) V(3)
* .PRINT TRAN V(6) V(3)
.AC DEC 200 IOK 10MEG
.PRINT AC V(3) VOB(3) V(2) V(I) V(4)
.ENO
```

Figure A.9   Continuation of Listing - 4

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